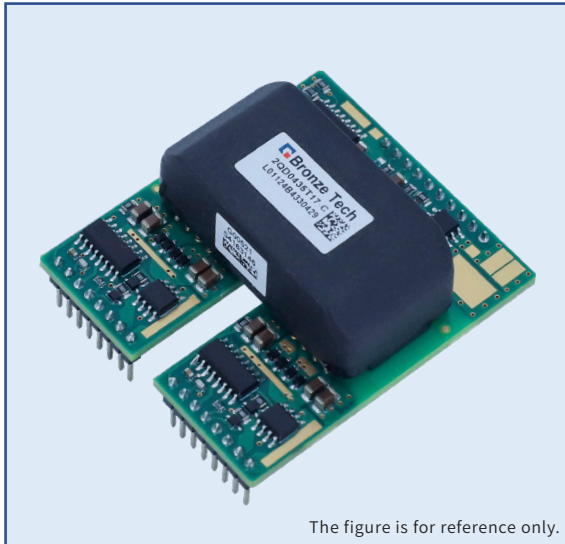


2QD0435T17-C-xx Gate Driver Core



Features

- Dual-channel IGBT gate driver core
- Blocking voltage up to 1700V
- Peak current $\pm 35A$, 4W output power per channel
- Up to 5000V isolation voltage
- Direct/half-bridge mode available
- Primary/secondary side undervoltage lockout
- IGBT short-circuit protection integrated
- Advanced active clamping integrated

RoHS
COMPLIANT

KEY PARAMETERS

V_{CC}	15V
V_G	+15V, -10V
P, MAX	4W
I_G , MAX	$\pm 35A$
f_s , MAX	100kHz
T_A	-40°C ~85°C
Isolation Voltage	5000Vac

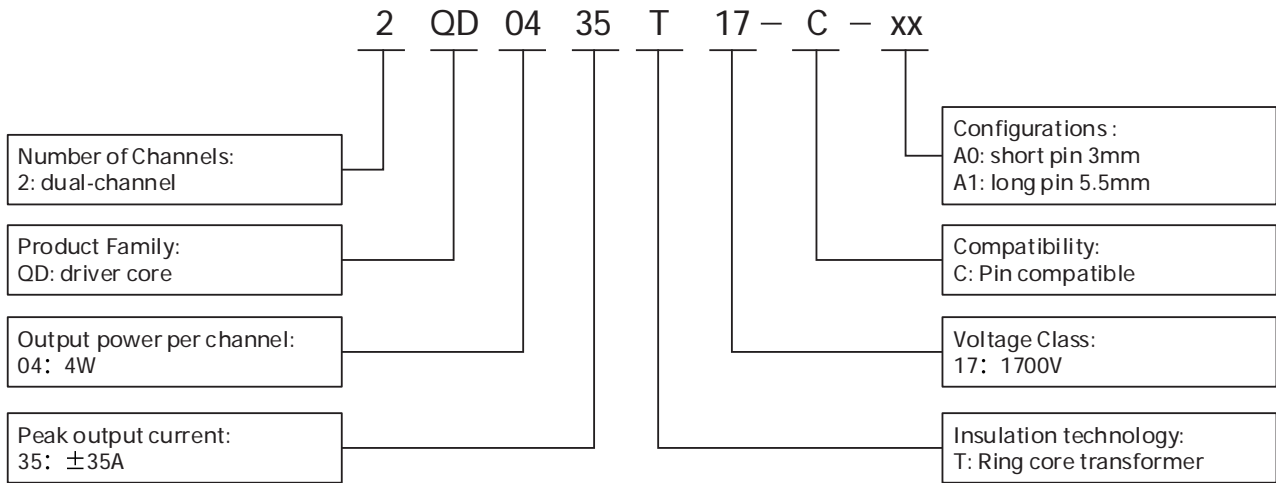
Description

2QD0435T17-C-xx is a high power, dual-channel compact gate driver core designed for high reliability applications based on the ASIC chipset developed by Bronze Technologies. 2QD0435T17-C-xx can be used for IGBT modules with a blocking voltage up to 1700V. It can be applied to various topologies by adding proper peripheral circuitry.

Typical Applications

- Energy storage converters
- Wind power converters
- PV inverters
- Motor Drives
- SVG
- APF

Nomenclature



Block Diagram Of Driver Core

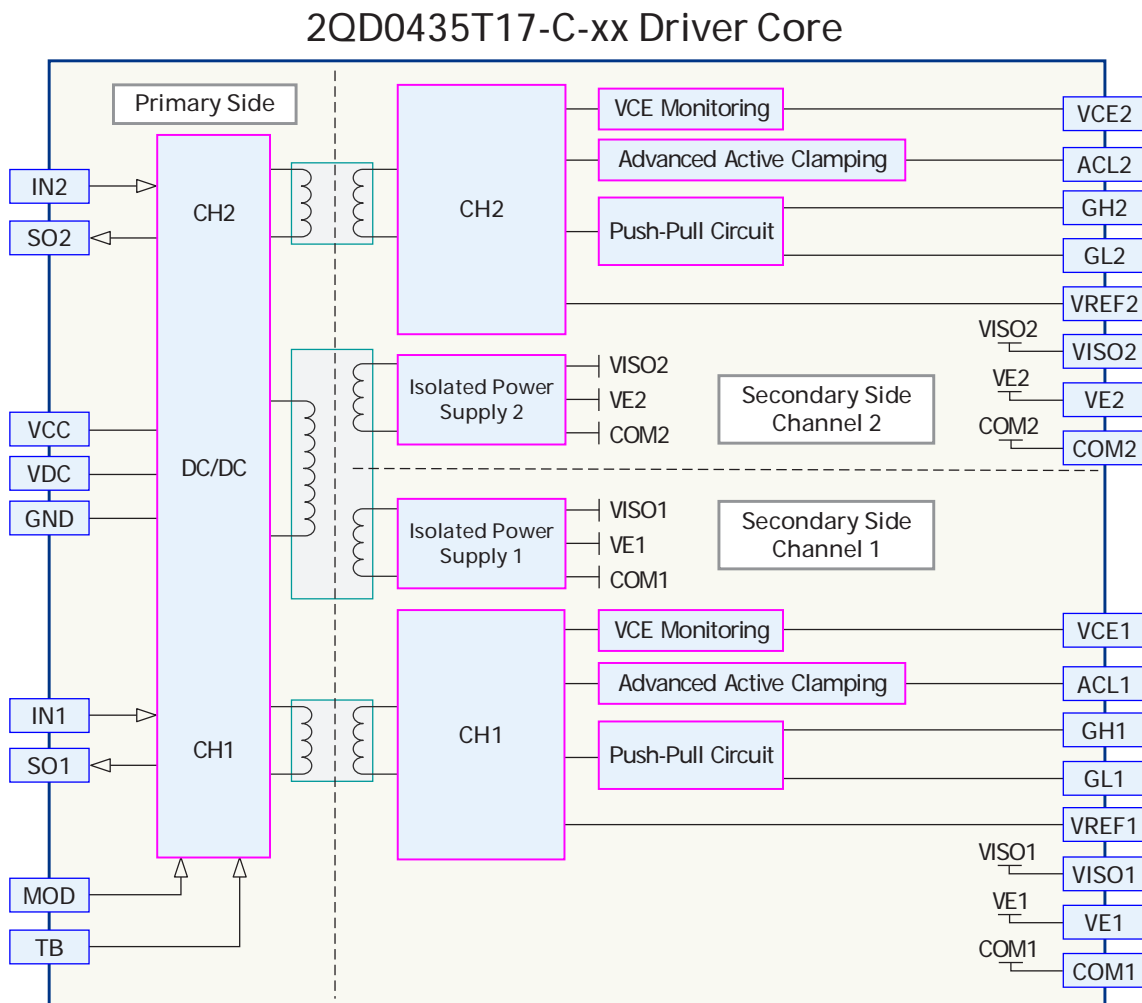


Figure 1. Block diagram of 2QD0435T17-C-xx

Recommended Circuitry

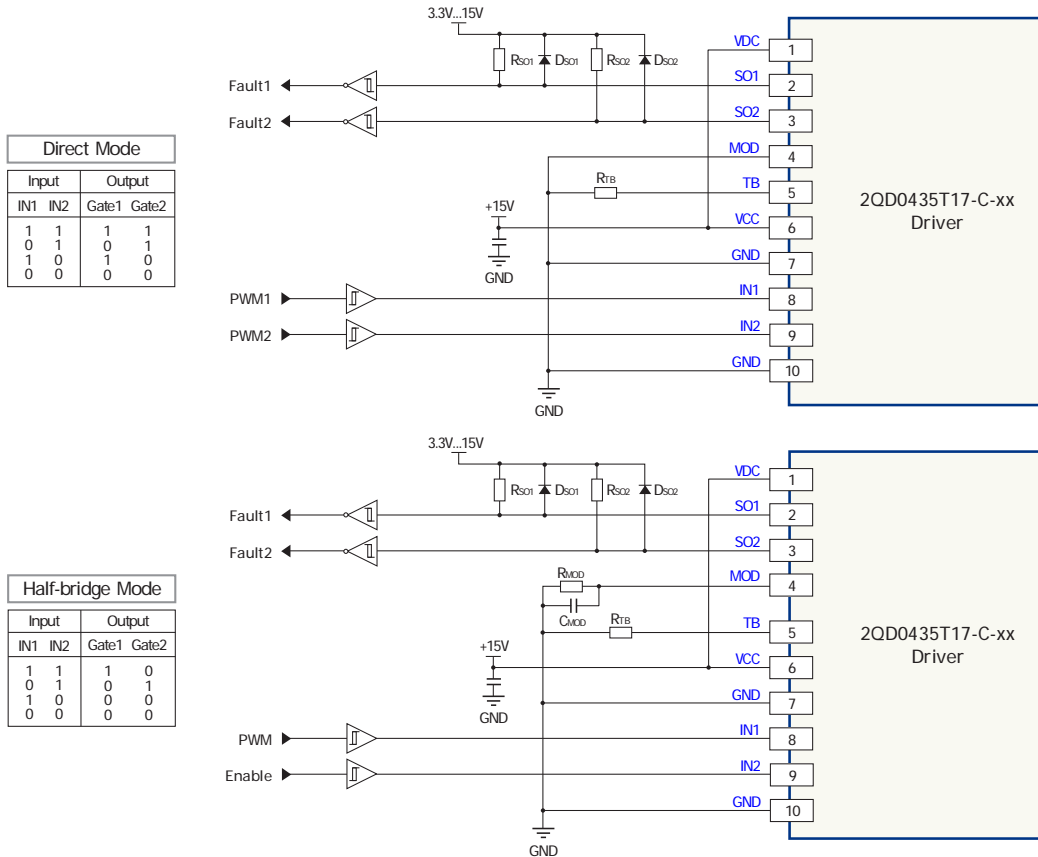


Figure 2. Recommended user interface of 2QD0435T17-C-xx (Primary Side)

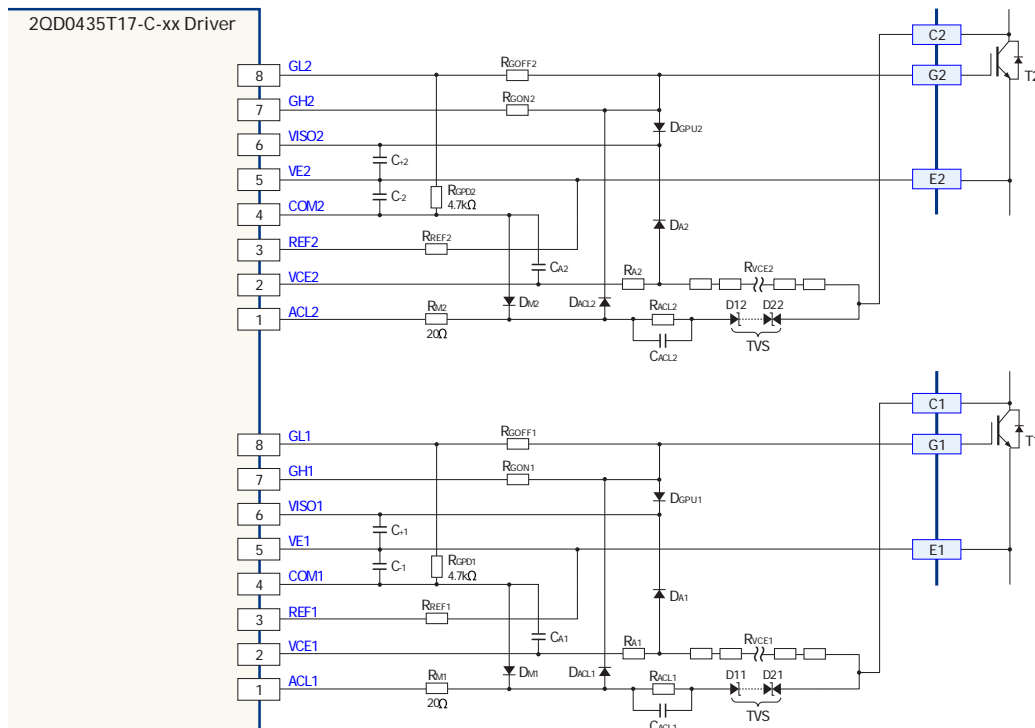


Figure 3. Recommended user interface of 2QD0435T17-C-xx (Secondary side)

Pin Designation

P1 Terminal

Pin	Symbol	Description
1	ACL1	Advanced Active Clamping feedback channel 1 ¹⁾
2	VCE1	VCE sense channel 1 ²⁾
3	REF1	Set V _{CE} detection threshold voltage channel 1 ³⁾
4	COM1	Negative secondary side power supply channel 1 ⁴⁾
5	VE1	Emitter channel 1 ⁵⁾
6	VISO1	Positive secondary side power supply channel 1 ⁶⁾
7	GH1	Gate high channel 1, gate ON output ⁷⁾
8	GL1	Gate low channel 1, gate OFF output ⁸⁾

P2 Terminal

Pin	Symbol	Description
1	ACL2	Advanced Active Clamping feedback channel 2 ¹⁾
2	VCE2	VCE sense channel 2 ²⁾
3	REF2	Set VCE detection threshold channel 2 ³⁾
4	COM2	Negative secondary side power supply channel 2 ⁴⁾
5	VE2	Emitter channel 2 ⁵⁾
6	VISO2	Positive secondary side power supply channel 2 ⁶⁾
7	GH2	Gate high channel 2, gate ON output ⁷⁾
8	GL2	Gate low channel 2, gate OFF output ⁸⁾

- Note:
- 1) Left open if unused. For the detailed configuration, see the section "Active Clamping".
 - 2) The desaturation detection pin of the driver. For details, see the section "IGBT Short-Circuit Protection".
 - 3) Threshold voltage setting pin for the internal desaturation detection comparator of the driver. For details, see the section "IGBT Short-Circuit Protection".
 - 4) Driver negative supply. Extra blocking capacitors can be connected externally.
 - 5) Connected to blocking capacitor and emitter of the power device.
 - 6) Driver positive supply. Extra blocking capacitors can be connected externally.
 - 7) Gate high pin is connected to the external turn-on resistor R_{GONx}. It is pulled to VISOx for ON state and becomes high impedance for OFF state.
 - 8) Gate low pin is connected to the external turn-off resistor R_{GOFFx}. It is pulled to COMx for OFF state and becomes high impedance for ON state.

P3 Terminal

Pin	Symbol	Description	Pin	Symbol	Description
1	VDC	15V for DC/DC converter ¹⁾	6	VCC	15V for primary side electronics
2	SO1	Status output channel 1	7	GND	Ground
3	SO2	Status output channel 2	8	IN1	Signal input channel 1
4	MOD	Mode selection (direct/half-bridge mode)	9	IN2	Signal input channel 2
5	TB	Set blocking time ⁴⁾	10	GND	Ground

Note: 1) A stable 15V DC power supply is recommended. Be sure to have enough blocking capacitors to avoid voltage dips.

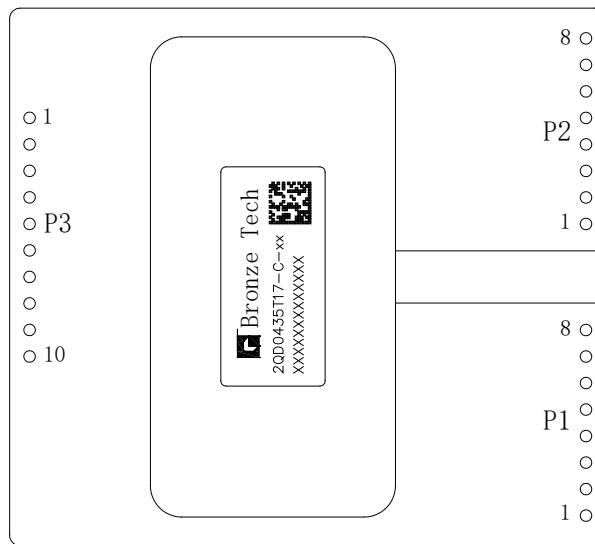


Figure 4. 2QD0435T17-C-xx pin layout

Specifications

Absolute Maximum Ratings

PARAMETER	REMARKS	MIN	MAX	UNIT
Supply voltage V_{CC}, V_{DC}	VCC, VDC to GND	0	16	V
Logic input and output voltages	Primary side, to GND	0	VCC	
SOx current	Failure condition, total current		20	mA
Output power per channel	Operating temperature $\leq 85^\circ\text{C}$		4	W
Gate peak current ¹⁾		-35	35	A
External gate resistance	Turn-on and turn off	0.5		Ω
Operating voltage			1700	V
Average supply current I_{DC} ²⁾			620	mA
Switching frequency			100	kHz
Operating temperature T_A		-40	85	$^\circ\text{C}$
Storage temperature T_s		-40	85	

Note: 1. It is an absolute value and only valid for short pulses.
 2. The average current may exceed the specified maximum value during transient (e.g. power supply start up). This short overload is allowed as long as the temperature rise after the transient does not exceed the thermal limitation.

Power supply and monitoring

Operating temperature $T_A=25^\circ\text{C}$, $V_{CC}=V_{DC}=15\text{V}$,
 unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITONS	MIN	TYP	MAX	UNIT
Supply voltage V_{CC}, V_{DC}		VCC, VDC to GND, recommended value	14.5	15	15.5	V
Supply current I_{CC}		No load, $f_{SW}=0\text{Hz}$		11		mA
Supply current I_{DC}	$R_{GON}=1\Omega, R_{GOFF}=1\Omega$	No load, $f_{SW}=5\text{kHz}$, 50% duty cycle		49		
		No load, $f_{SW}=10\text{kHz}$, 50% duty cycle		53		
		Load capacitance 100nF, $f_{SW}=10\text{kHz}$, 50% duty cycle		147		
Secondary-side full voltage V_{CCO}		VISOx to COMx, no load	24	25	26	V
Secondary-side positive voltage V_+		VISOx to VEx, no load	14.5	15	15.5	
Secondary-side negative voltage V_-		COMx to VEx, no load	-10.5	-10	-9.5	
Primary side supply UVLO threshold Voltage ¹⁾	Set fault V_{CCUV+}	VCC-GND	12	12.5	13	V
	Clear fault V_{CCUVR+}		13	13.5	14	
	Monitoring hysteresis			1		
Secondary side positive supply UVLO threshold voltage ¹⁾	Set fault V_{UV+}	VISOx-VEx	11.5	12	12.5	
	Clear fault V_{UVR+}		12	12.5	13	
	Monitoring hysteresis			0.5		

(Continued)

Secondary side negative supply UVLO threshold voltage ¹⁾	Set fault V_{UV-}	VEx-COMx	4	4.4	5	V
	Clear fault V_{UVR-}		4	4.5	5	
	Monitoring hysteresis		0.1			

Note: 1. See the section "Power Supply and Monitoring" for timing diagram of the UVLO.

Logic Input and Output

Operating temperature $T_A=25^\circ\text{C}$, $V_{CC}=V_{DC}=15\text{V}$, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current I_{IN}		$V_{IN} > 3\text{V}$		180		μA
IN1, IN2 Input voltage V_{IN}	Turn-on threshold V_{INH}			2.4		V
	Turn-off threshold V_{INL}			1.6		
Mode selection resistor ¹⁾	Direct mode	MOD shorted to GND		0		k Ω
	Half-bridge mode	MOD connected to GND via a resistor	72	150	182	
Blocking time setting resistor R_{TB} ²⁾			75		185	
SO output voltage V_{SO} ³⁾	Normal state	$R_{SOx}=4.7\text{k}\Omega$ pulled up to VCC		15		V
	Blocking state	$I_{SOx} < 20\text{mA}$			0.7	

Note: 1. Mode selection and dead time configuration resistor. For details, see the section "Transmission Logic and Mode Selection".
 2. The Blocking time configuration resistor. For details, see the section "Blocking Time Setting".
 3. SOx outputs have open-drain transistors, users need to add the pull-up resistor R_{SOx} externally. For more details see the section "Status Output Signal".

Gate Drive Output

Operating temperature $T_A=25^\circ\text{C}$, $V_{CC}=V_{DC}=15\text{V}$, unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage	ON-State, V_{GHx} , GHx to Ex	No load		15		V
	OFF-State, V_{GLx} , GLx to Ex	No load		-10		
		Output power 4W			-9.5	
Gate peak current $I_{G\text{ peak}}$	Source current	$R_{GON}=0.5\Omega$, $R_{GOFF}=0.5\Omega$, load capacitance 2.47 μF			35	A
	Sink current		-35			
Blocking capacitance for V+ ¹⁾		VISOx to VEx		9.4		μF
Blocking capacitance for V- ¹⁾		COMx to VEx		9.4		

Note: 1. External blocking capacitors are required to be placed between VISOx and VEx as well as between VEx and COMx for gate charges above 3 μC . Ceramic capacitors are recommended. A minimum external blocking capacitance of 3 μF is recommended for every 1 μC of gate charge beyond 3 μC . Insufficient external blocking capacitance may lead to reduced driver efficiency and thermal overload.

Short Circuit Protection

Operating temperature $T_A=25^\circ\text{C}$, $V_{CC}=V_{DC}=15\text{V}$,
 unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current through pin REFx (internal current source)	$R_{REF}<70\text{k}\Omega$		150		μA
Blocking time $t_B^{1)}$	$R_{TB}=150\text{k}\Omega$		95		ms
	TB shorted to ground		10		μs
Transmission delay of fault state $t_{SO}^{2)}$	Secondary-side short-circuit protection action to fault status output		600		ns
Note: 1. For other blocking time configurations, see the section "Blocking Time Setting". 2. Propagation delay time is from the secondary-side protection action to the primary-side SOx pin pulled down.					

Timing Characteristics

Operating temperature $T_A=25^\circ\text{C}$, $V_{CC}=V_{DC}=15\text{V}$,
 unless otherwise specified, tested along with the recommended interface circuitry.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation delay $t^{1) 3)}$	Turn-on delay $t_{d(on)}$		215		ns	
	Turn-off delay $t_{d(off)}$	$R_{GON}=1\Omega$, $R_{GOFF}=1\Omega$, no load		230		
Jitter of turn-on delay	$R_{GON}=1\Omega$, $R_{GOFF}=1\Omega$, no load		± 5			
Jitter of turn-off delay			± 5			
Output rise time $t_r^{2) 3)}$				32		
Output fall time $t_f^{2) 3)}$				32		
Dead time $DT^{4)}$	Half-bridge mode, $R_{MOD}=150\text{k}\Omega$		3		μs	
Jitter of dead time			± 50		ns	
Note: 1. The delay time is measured between 50% of the input signal and 10% (90%) voltage swing of V_{GHx} (V_{GLx}). The delay time is independent of the output load. 2. Output rise (fall) time is measured at GH (GL) at the driver side of the gate resistor R_{GONx} (R_{GOFFx}) between the 10% and 90% of the nominal voltage swing. The time constant of the output load capacitance in conjunction with the present gate resistors leads to an additional delay at the load side of the gate resistors. 3. The voltage swing is the difference between the output voltage at ON and OFF state on the GH or GL pins, referred to Ex. 4. For dead time configuration see section "Transmission Logic and Mode Selection / Half-Bridge Mode".						

Electrical Isolation

Operating temperature $T_A=25^\circ\text{C}$, unless otherwise specified, tested along with the standard peripheral circuitry.

PARAMETER		VALUE	UNIT
Isolation Voltage (50Hz, 1s, RMS value)	Primary to Secondary side	5000	V
	Secondary to Secondary side	4000	
Primary to secondary side ¹⁾	Coupling capacitance	27	pF
	Clearance distance	16.5	mm
	Creepage distance	16.5	
Secondary to secondary side ¹⁾	Clearance distance	6.3	mm
	Creepage distance	13	

Note: 1. Clearance and creepage distances are designed according to IEC 61800-5-1.

EMC

Ambient temperature $T_A=25^\circ\text{C}$, tested along with the standard peripheral circuitry.

PARAMETER		VALUE	UNIT
ESD immunity (IEC 61000-4-2)	Contact discharge	± 4	kV
	Air discharge	± 8	
Electrical fast transient/burst immunity ¹⁾ (IEC 61000-4-4)		± 4	
Impulse magnetic field immunity (IEC 61000-4-9)		± 2000	A/m

Note: 1. Tested on power ports.

Ordering Information

Part Number	IGBT Voltage	Pin Length	Conformal Coating
2QD0435T17-C-A0	< 1700V	3mm	Yes
2QD0435T17-C-A1		5.5mm	Yes

Function Description

Power Supply And Monitoring

The DC/DC circuitry of the driver provides galvanic isolation between external power supply and gate driving circuit. Supply monitoring circuitry is deployed for the primary-side and two secondary-sides of the drive for undervoltage lockout.

Note: A stable primary side supply voltage is required.

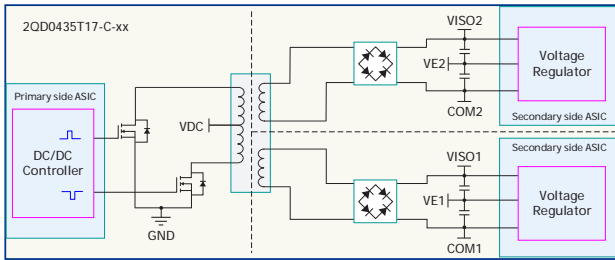


Figure 5. Power supply circuitry

Primary Supply Monitoring:

The supply voltage V_{CC} is monitored on the primary-side for undervoltage lockout (UVLO). When V_{CC} drops to the UVLO threshold V_{CCUV+} , UVLO is triggered, two secondary-side outputs are locked in off state and keep the IGBT off. Meanwhile, the fault signals SO1 and SO2 are pulled down.

When V_{CC} returns to the UVLO clear fault threshold V_{CCUVR+} , the driver continues to maintain the lockout state for a period t_B , then exit the lockout state and pulls up fault signals SOx.

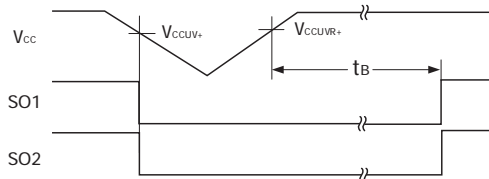


Figure 6. Primary-side UVLO logic

Secondary Side Supply Monitoring:

The driver also monitors the secondary side power supply to ensure proper operation of the IGBT. To describe the undervoltage protection on the secondary side, an example is the case in which the secondary side full voltage V_{CCO} (VISO to COM) drops from the rated value to 0V:

- 1) At first the positive voltage V_+ (VISO to VE) is held constant on the nominal value, while the negative voltage V_- (COM to VE) deviates from the nominal value towards zero along with the decreasing V_{CC} .
- 2) As soon as V_- reaches -5V, V_- is held constant and V_+

starts to fall towards zero if V_{CC} further collapses.

- 3) When V_+ reaches the set fault threshold V_{UV+} , UVLO protection is initiated. The IGBT is turned off and held in off state, meanwhile a set fault signal is transmitted to the primary side and asserts SOx pin immediately.
- 4) The counting of t_B starts when a UV fault is detected. This is different from the primary side supply voltage monitoring, where the counting of t_B starts after UV fault is cleared. If a new fault is detected before t_B of the previous fault elapses, t_B is recounted from the new fault.
- 5) When V_{CC} rises again, the driver firstly restores V_+ .
- 6) If V_+ further increases and reaches its nominal value, V_+ is held constant and V_- starts to recover towards its nominal value.

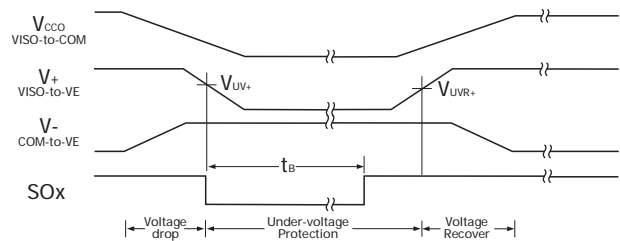


Figure 7. Secondary-side UVLO logic

Transmission Logic and Mode Selection

The driver can operate in direct or half-bridge mode. Operation mode of the driver can be selected by configuring the connection of the MOD pin.

Direct Mode:

If the MOD pin is shorted to ground, direct mode is selected. In direct mode, the two channels are independent. Input IN1 determines the output of Channel 1, while input IN2 determines that of Channel 2. A logic high turns on the corresponding IGBT, while a logic low turns it off.

Note: In direct mode, make sure to add a proper dead time in the input signals to avoid shoot-through of the two switches in a bridge.

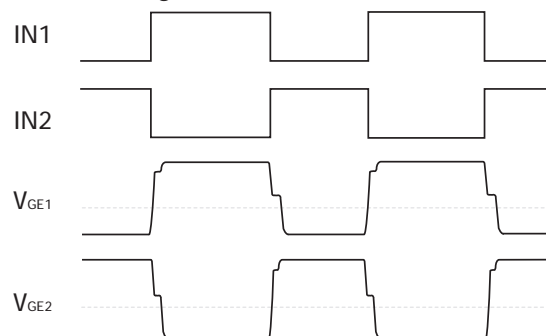


Figure 8. Transmission logic in direct mode

Half-Bridge Mode:

If the MOD pin is connected to ground via a resistor, the driver operates in half-bridge mode. In this mode, the IN1 serves as PWM signal and the IN2 as enabling signal.

When IN2 is low, both channels are locked in off state. If IN2 is high, both channels are enabled. The gate output signals of both channels are determined by IN1. At the transition of IN1 from low to high, the gate signal of Channel 2 is turned off immediately. After the dead time DT elapses, the gate signal of Channel 1 is turned on. At the transition of IN1 from high to low, the gate signal of Channel 1 is turned off immediately. After the dead time DT elapses, the gate signal of Channel 2 is turned on.

The dead time is set by an external resistor R_{MOD} connected between MOD pin and GND. The following formula defines the relationship between R_{MOD} and the dead time DT:

$$R_{MOD} [k\Omega] = 30.9 \cdot DT[\mu s] + 55.9$$

$$0.5\mu s < DT < 4.1\mu s, 72k\Omega < R_{MOD} < 182k\Omega$$

When R_{MOD}=150kΩ, the dead time DT is around 3.0us.



Figure 9. Transmission logic in half-bridge mode

Status Output Signal

When no fault is detected, Q_{SOx} keeps off, the outputs SOx have high impedance. When a fault is detected, the corresponding SOx is pulled down to ground.

It is recommended to mount external pull-up resistors as demonstrated in the diagram of recommended user interface of 2QD0435T17-C-xx. There the diodes D_{SOx} are only required when using 3.3V input logic level.

In a fault condition, the maximum SOx current must not exceed 20mA.

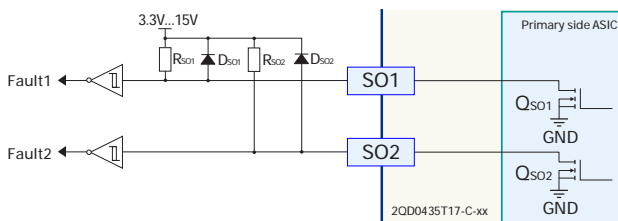


Figure 10. Block diagram and recommended circuit of status signal output

SO1 and SO2 can be connected together to provide protection information of the entire driver. However, for fast and precise fault diagnosis, it is recommended to detect the information independently.

Blocking Time Setting

The blocking time t_B can be configured by an external resistor R_{TB} between TB pin and GND.

The following formula describes the relationship between t_B and R_{TB} (at typical values).

$$R_{TB}[k\Omega] = t_B[ms] + 55$$

$$(75k\Omega \leq R_{TB} \leq 185k\Omega, 20ms \leq t_B \leq 130ms)$$

Note: R_{TB} should not be smaller than 75kΩ, which means the blocking time t_B cannot be shorter than 20ms, otherwise the blocking time t_B will be inaccurate and unstable. If TB pin is shorted to ground, t_B is fixed to 10us.

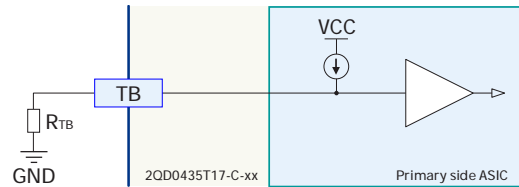


Figure 11. Blocking time setting

IGBT Turn-On and Turn-Off

To turn on the IGBT, Q_{ON} inside the ASIC of the driver is turned on, and Q_{OFF} is turned off. The gate resistor R_{GON} is pulled up to charge the gate and the IGBT is turned on.

To turn off the IGBT, Q_{OFF} inside the ASIC of the driver is turned on, and Q_{ON} is turned off. The gate resistor R_{GOFF} is pulled down to COMx to discharge the gate and the IGBT is turned off.

The driver allows user to set the turn-on and turn-off resistors independently. It is recommended to connect a resistor of 4.7kΩ between GLx and COMx. It is also recommended to add a clamping diode D_{G_PUx}, which prevents overvoltages of the gate and protect the IGBT module.

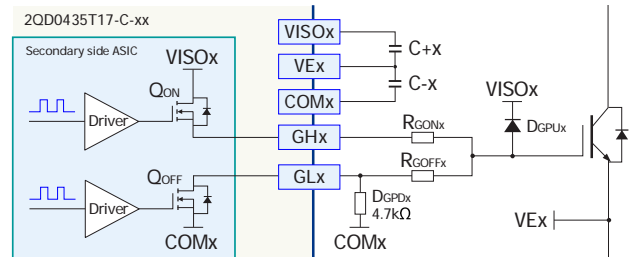


Figure 12. Gate drive output circuitry

Active Clamping

Fast IGBT turn-off may lead to voltage spike, which is critical when DC-link voltage and load current are high. Voltage spikes can cause damage to the IGBT. The turn-off voltage spike is mainly due to the stray inductance L_s and the slew rate of the IGBT turn-off current di/dt . By adjusting the turn-off gate resistor R_{GOFF} , the di/dt can be reduced and the voltage overshoot is reduced. However, the impact of L_s is inevitable. It can be more pronounced under high current in short circuit or overload. It is recommended to add active clamping circuitry to effectively prevent the overvoltage damage on IGBT. A feedback path from the IGBT collector to the gate is established using transient voltage suppressor devices(TVS). When the V_{CE} peak voltage exceeds the breakdown threshold, the TVS chain will break through and the current through it will charge the IGBT gate, which turns on the IGBT partially and suppresses the excessive V_{CE} of the IGBT.

Anti-parallel diodes of the IGBT module have forward recovery effect when they are turned on, to avoid negative current flows through the TVS chain, at least one bidirectional TVS must be used for each channel. The recommended breakdown thresholds for the application circuit of the driver are shown in the table below.

DC Link Voltage	TVS Chain Breakdown Threshold @ 25°C	D1x	D2x
800V	912V	5 x SMBJ130A	1 x SMBJ130CA
1200V	1320V	5 x P6SMB220A	1 x PB6MB220CA

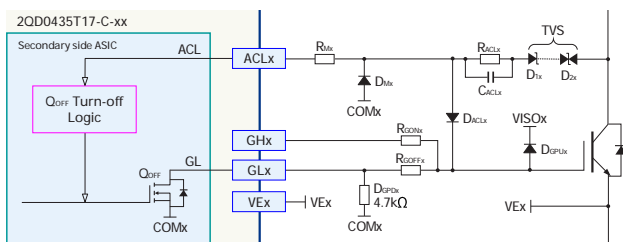


Figure 13. Recommended circuitry for active clamping

IGBT Short-Circuit Protection

The V_{CE} detection circuitry is used for IGBT short-circuit protection. The detection of two channels are independent from each other. The short-circuit detection

is only valid when the IGBT is turned on. When the IGBT is in off state, the input signal turns on Q_{CEx} and clamps V_{CEx} to $COMx$. In this case, the comparator outputs logic low.

The threshold of comparator is set by external resistors R_{REFx} connected to $REFx$ pin. Inside $REFx$ pin there a built-in current source of 150uA, an external resistor R_{REFx} 68kΩ configures a threshold voltage of 10.2V for the short circuit detection.

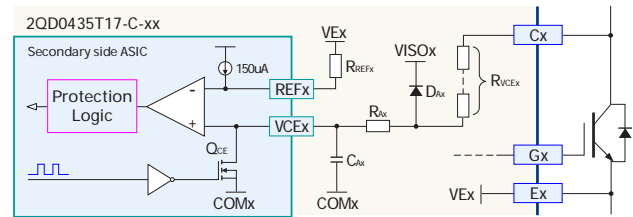


Figure 14. Block diagram and recommended circuit for short-circuit protection

Normal Turn-on:

When the logic input will turn on the IGBT, Q_{CE} is firstly turned off and releases the clamping of V_{CEx} clamping. At this moment, IGBT is still in off state and V_{CE} is high. C_{Ax} capacitor is charged through the resistor chain composed of R_{VCEx} and R_{Ax} , V_{CEx} rises. Then the IGBT is turned on, V_{CE} quickly drops to saturation voltage V_{CE-SAT} and V_{CEx} reaches V_{CE-SAT} .

The response time is the time interval between turn-on of the IGBT and the collector voltage is started to be measured, within the response time, V_{CE} is deactivated. The response time can be determined by configuring the capacitor C_{Ax} following the table in below ($R_{VCEx}=1.8M\Omega$, $R_{Ax}=120k\Omega$, DC link voltage >550V).

Table 1. Typical response time under different C_{Ax} and R_{REFx}

C_{Ax} [pF]	R_{REFx} [kΩ] / V_{REFx} [V]	Response time [μs]
15	68/10.2	6.1
22	68/10.2	7.5
33	68/10.2	9.4
47	68/10.2	11.6

Be sure to configure a response time that is shorter than the maximum allowed short-circuit duration of the IGBT.

As V_{CE-SAT} is significantly lower than the protection threshold V_{REF} , the comparator does not flip over and the protection is not initiated.

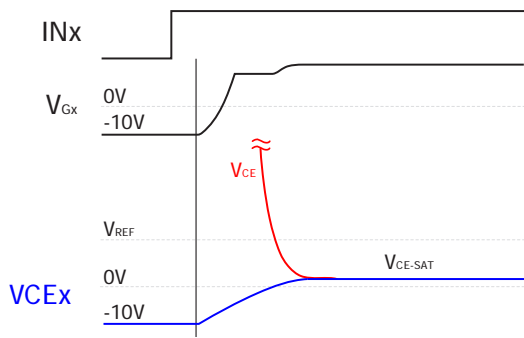


Figure 15. VCEx signal waveform at normal turn-on

Class I Short- Circuit Protection:

When Class I short circuit (bridge shoot-through) occurs, due to the rapid increase of the short circuit current, the IGBT desaturates and result in rapidly increased V_{CE} . C_{Ax} is charged and V_{CEx} rises until it is clamped at V_{ISOx} . During this process, V_{CEx} exceeds V_{REF} and the comparator's output flips, which consequently triggers the short-circuit protection.

The short-circuit protection logic turns off the IGBT immediately to ensure its safety. At the same time, set fault signal is sent to the primary side to pull down the SOx pin, so as to alert a fault state. The channel is locked in fault state for a period t_B before recovering to the normal state. The protection circuits of the two channels are independent from each other. Therefore, when short-circuit protection is initiated on one channel, the other channel remains operating normally. It is recommended to check the SOx signal timely and activate system lockout when necessary.

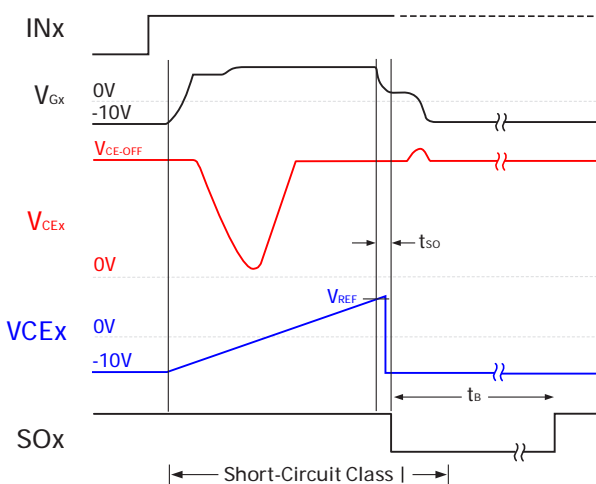


Figure 16. Logic of class I short-circuit protection

Class II Short-Circuit Protection:

When a Class II short circuit (e.g. phase to phase short circuit) occurs, the current ramps up slowly as the short circuit impedance is relatively high. The IGBT still enters saturation state normally. As the short-circuit current increases, V_{CE} increases gradually until it exceeds the protection threshold, then the driver initiate short-circuit protection. The response time in Class II short-circuit protection is longer than that of Class I. In another case, if bridge shoot-through occurs under low DC-link voltage, the short circuit current is low and also resulting in increased protection response time.

Note: When a Class II short circuit occurs, the short circuit impedance varies greatly, which leads to uncertain timing of IGBT desaturation. Therefore, before the protection is initiated, the IGBT may have been already damaged by a considerable sum of heat accumulated. In this case, the driver's short-circuit protection cannot guarantee the intactness of the IGBT. Extra overcurrent protection measures have to be introduced.

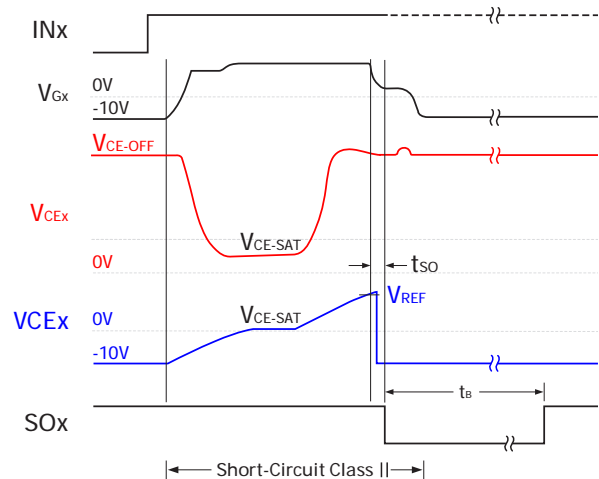


Figure 17. Logic of class II short-circuit protection

Mechanical Dimensions

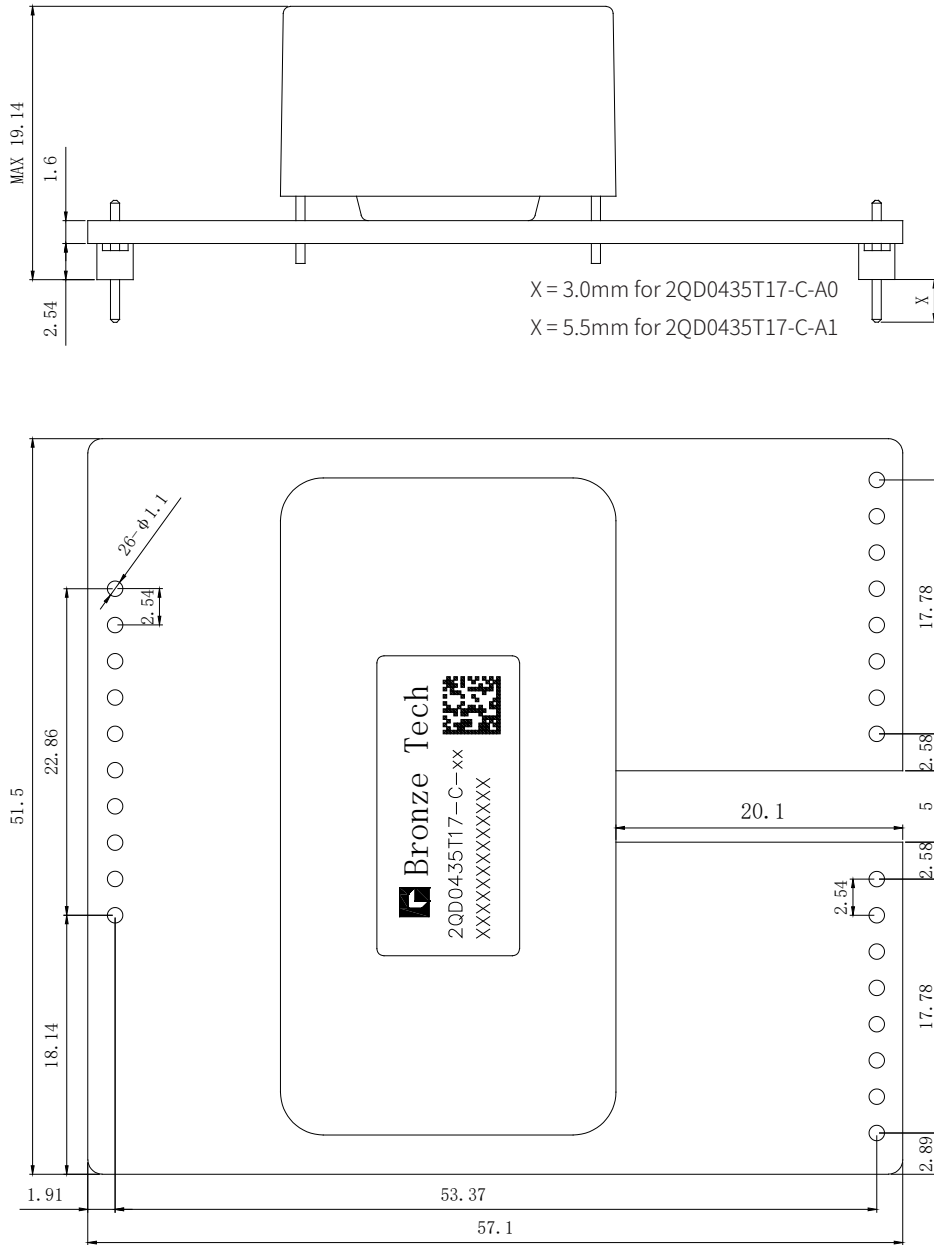


Figure 18. Mechanical drawing of 2QD0435T17-C-xx

- Note: 1)Legend unit: mm.
 2)The margin tolerance conforms with the ISO 2768-1, Class f.
 3) PCB Thickness Tolerance $\pm 10\%$.
 4)The primary side and secondary side pin grid is 2.54mm with a pin cross section of 0.64mmx0.64mm. Recommended diameter of solder pads is 2mm and diameter of drill holes is 1mm.

Revision History

REVISION	NOTES	DATE
V1.0	Initial release	12-Jun-2019
V1.1	Modified data	19-Jun-2019
V1.2	Updated introduction	20-Jul-2019
V1.3	Updated the manual template	04-Nov-2019
V1.4	The manual template updated, and the content standardized	18-Aug-2021
V1.5	Content updated after introduction of 2nd generation ASIC	23-Sep-2023
V1.6	Updated figures and short circuit protection response time	25-Dec-2023
V1.6.1	Notes on optimising mechanical dimensions	28-Dec-2024

Precautions

- All operations on the IGBT module and driver shall conform with the electrostatic-sensitive device (ESD) protection requirements stipulated in IEC 60747-1/IX or EN100015.
- To protect ESDs, IGBT module and driver operation, including the operation sites and tools, must conform with these standards.



The IGBT and driver may be damaged due to negligence in ESD protection.

- Before powering on the driver, make sure that the driver and control board are connected correctly, without empty connection, false connection, or false soldering.
- After the driver is installed, its surface voltage to the ground may exceed the safety voltage. Therefore, do not touch it with bare hands.



Operations may involve life hazards. Be sure to follow the corresponding safety protocols !

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