BTD3011x

Single-Channel Isolated Gate Driver

1.Features

- Isolation voltage up to 5000Vrms
- Peak output current up to ±15A
- CMTI=150kV/μs Minimum
- Maximum switching frequency 75kHz
- Secondary-side supply up to 28V
- Primary-side and secondary-side power supply undervoltage lockout (UVLO)
- Compatible with 3.3V, 5V input
- Short circuit protection and soft shut down integrated
- Voltage regulator integrated for secondary-side power supply
- SOW-16 (wide-body) package
- Operating Temperature -40~125°C

2.Applications

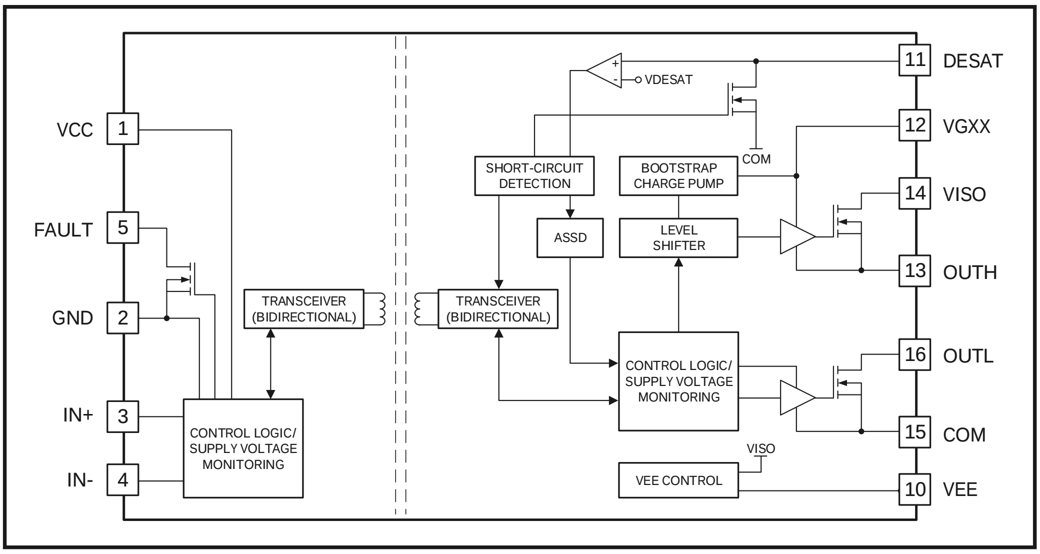
- Industrial motor drives
- EV motor drives
- PV inverters
- Energy storage inverters

3.Description

BTD3011x is a single channel gate driver with galvanic isolation provided using magnetic coupling. The peak output drive current is ±15A. The SOW-16 package enables an isolation voltage of 5000Vrms. Short circuit protection, soft shut down and primary/secondary side undervoltage lockout (UVLO) are provided. Voltage regulator is integrated for the secondary-side supply. the peripheral circuit design is significantly simplified.

RoHS
COMPLIANT

4.Functional Block Diagram



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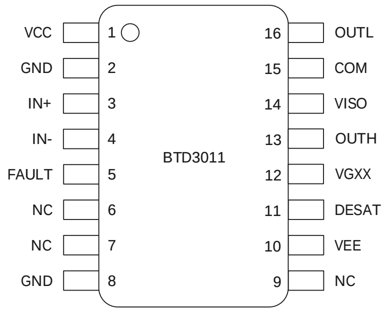
5.Product Information

Part No.	Functions	Isolation Voltage	Operating Temperature	Package	Package Material	Quantity	Marking
BTD3011R	Short circuit protection, soft shut down, primary/secondary side UVLO, voltage regulator for secondary-side power supply	5000Vrms	-40~125°C	SOW-16	Tape & Reel	1500pcs/ Reel	BTD3011

6.Pin Configuration and Functions

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	VCC	P	Primary-side supply voltage	
2	GND	G	Primary side ground	
3	IN+	I	Non-inverted input	
4	IN-	I	Inverted input	
5	FAULT	O	Fault state output	
6	NC	-	No internal connection	
7	NC	-	No internal connection	
8	GND	G	Primary side ground	
9	NC	G	No internal connection	
10	VEE	G	Connected to IGBT emitter/MOSFET source	
11	DESAT	I	Desaturation monitoring voltage input	
12	VGXX	P	Bootstrap and charge pump supply voltage source	
13	OUTH	O	Driver output turn-on connection	
14	VISO	P	Secondary-side positive power supply rail	
15	COM	P	Secondary-side negative power supply rail	
16	OUTL	O	Driver output turn-off connection	

(1) P=Power, G=Ground, I=Input, O=Output

7.Specification Parameters

7.1 Absolute Maximum Ratings

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Input bias pin supply voltage, V_{CC}	VCC-GND	-0.5	6.5	V
Secondary-side total supply voltage, V_{TOT}	VISO-COM	-0.5	30	
Secondary-side positive supply voltage	VISO-VEE	-0.5	17.5	
Secondary-side negative supplyvoltage	VEE-COM	-0.5	15	
Logic input voltage	IN+, IN- to GND	-0.5	V_{CC}+0.5	
Logic output voltage	FAULT to GND	-0.5	V_{CC}+0.5	
DESAT pin voltage	DESAT-COM	-0.5	V_{TOT}+0.5	
Switching frequency, f_S	-	-	75	kHz
Operating junction temperature, T_J	-	-40	150	°C
Storage temperature, T_S	-	-40	150	
Soldering temperature (10s), T_L	-	-	300	
Input power dissipation P_P	V_{CC}=5V, V_{TOT}=28V, T_A=25°C , f_S=75kHz		188	mW
Output power dissipation P_S			1602	
Total IC power dissipation P_{DJS}			1790	
ESD	Human body model (HBM)	±2000		V
	Charged device model (CDM)	±1000		

Note: The above are stress levels only.Devices are not recommended to operate under these or any other conditions beyond these values.Prolonged operation under the absolute maximum rating may affect the reliability of the device, and in severe cases it may cause permanent damage to the devices.

7.2 Thermal Resistance Information

SYMBOL	DESCRIPTION	SOW-16	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.58	°C /W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.52	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.47	
ψ_{JT}	Junction-to-top characterization parameter	31.47	
ψ_{JB}	Junction-to-board characterization parameter	41.69	

7.3 Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{CC}	Input supply voltage	4.75	5.25	V
V_{TOT}	Secondary-side total supply voltage, VISO-COM	22	28	
V_{IN}	Logic input voltage	0	VCC	
T_A	Operating ambient temperature	-40	125	°C

7.4 Electrical Characteristics

T_A=-40~125°C, V_{CC}=3.3 or 5V, VISO=25V, C_L=100pF.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC}	Primary side quiescent current	V_{IN}=0V	-	-	17	mA
I_{VISO}	Secondary side quiescent current	V_{IN}=0V	-	-	15	mA
PRIMARY SIDE UNDERVOLTAGE LOCKOUT						
V_{ON1}	Primary side position supply voltage monitoring threshold	Clear fault	-	4.3	4.65	V
V_{OFF1}		Set fault	3.85	4.2	-	
$V_{UV, HYS1}$		Hysteresis	-	0.1	-	
SECONDARY SIDE POWER SUPPLY						
$V_{ISO(HS)}$	Secondary side positive supply voltage regulation	21V ⩽ V_{ISO} ⩽ 30V, |I_{VEE}| ⩽ 1.5mA	14.5	15	15.5	V
$UVLO_{VISO}$	Secondary side positive supply voltage monitoring threshold	Clear fault	-	13.2	14.2	
		Set fault	11.2	12.2	-	
		Hysteresis	-	1.0	-	
$UVLO_{VEE}$	Secondary side negative supply voltage monitoring threshold	Clear fault	-	4.92	5.5	
		Set fault	4.67	4.90	-	
		Hysteresis	-	0.02	-	
I_{VEE+}	VEE source capability	V_{TOT}=15V, VEE-COM=0V	-	0.2	-	mA
		V_{TOT}=25V, VEE-COM=7.5V	-	3	-	
I_{VEE-}	VEE sink capability	V_{TOT}=25V, VEE-COM=12.5V	-	-3	-	
INPUT CHARACTERISTICS						
V_{IH}	Positive-going input threshold voltage (IN+, IN-)	-	1.7	2.0	2.3	V
V_{IL}	Negative-going input threshold voltage (IN+, IN-)	-	1.4	1.6	1.8	
V_{IN_HYS}	Input hysteresis voltage	-	0.1	-	-	
I_{IH}	High-level input leakage at IN+	INx=VCC	56	113	165	μA
OUTPUT CHARACTERISTICS						
I_{OH}	Peak output source current	IN+=HIGH, IN-=LOW	-	15	-	A
I_{OL}	Peak output sink current	IN+=LOW, IN-=HIGH	-	-15	-	
VISO-V_{OH}	Output voltage at high state (OUTx, OUTHx)	I_{OUT}=20mA, IN+=HIGH, IN-=LOW	-	-	0.04	V
V_{OL}-COM	Output voltage at low state (OUTx, OUTLx)	I_{OUT}=-20mA, IN+=LOW, IN-=HIGH	-	-	0.04	
R_{GHI}	Turn-on internal gate resistance	I(GH)=250mA, V_{IN+}=5V	-	0.3	1.2	Ω
R_{LHI}	Turn-off internal gate resistance	I(GL)=-250mA, V_{IN+}=0V	-	0.25	1.1	
SHORT CIRCUIT PROTECTION						
V_{DESAT}	DESAT detection level	DESAT-VEE, V_{IN+}=5V	9.5	10.5	11.5	V
I_{DESAT}	DESAT sink current	V_{DESAT}=10V, V_{IN+}=0V	4.5	5.5	6.5	mA
$I_{DES\ (BS)}$	DESAT bias current	V_{VCE}-V_{VEE}=4.5V, V_{IN+}=5V	-	-	1	μA
SWITCHING PARAMETERS						
t_{PLH}	Propagation delay from INx to OUTx rising edges	C_L=100pF	180	280	380	ns
t_{PHL}	Propagation delay from INx to OUTx falling edges	C_L=100pF	200	287	359	
t_r	Output rise time	C_L=10nF	-	50	100	
t_f	Output fall time	C_L=10nF	-	50	100	
t_{FAULT}	Faults propagation delay	-	-	190	750	
$t_{FAULT-pw}$	Fault signal pulse width	-	6.8	10	13.4	μs
t_{FSSD1}	ASSD rate of change	VGE from 14.5V to 14V		60		ns
t_{FSSD2}		VGE from 14.5V to 2.5V	1750	2760	3800	
CMTI	Common-mode transient immunity	INx fixed to GND or VCC, V_{CM}=1500V	-	150	-	kV/μs

7.5 SAFETY PARAMETERS

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLR	External clearance	-	8.5	-	-	mm
CPG	External creepage	-	8.5	-	-	
DTI	Distance through the insulation	-	21	-	-	μm
CTI	Comparative tracking index	DIN EN 60112	600	-	-	V
-	Overvoltage category per IEC 60664-1	Voltage rating ≤ 600Vrms	I-III	-	-	-
		Voltage rating ≤ 1000Vrms	I-II	-	-	
DIN V VDE 0884-11						
C_{IO}	Barrier capacitance, input to output	V_{IO}=0.4Vrms, f=1MHz, sine wave	-	1.2	-	pF
R_{IO}	Isolation resistance, input to output	Test voltage of 500V, T_A=25°C	10^{12}	-	-	Ω
		Test voltage of 500V, 100°C≤ T_A ≤ 125°C	10^{11}	-	-	
		Test voltage of 500V, T_A=150°C	10^{9}	-	-	
-	Pollution degree	-	-	2	-	-
UL1577						
V_{ISO}	Withstand isolation voltage	V_{TEST}=V_{ISO}, t=60 sec(qualification)； V_{TEST}=1.2×V_{ISO}, t=1 sec(100% production)	-	5000	-	Vrms

8.Parameter Testing

8.1 Propagation Delay

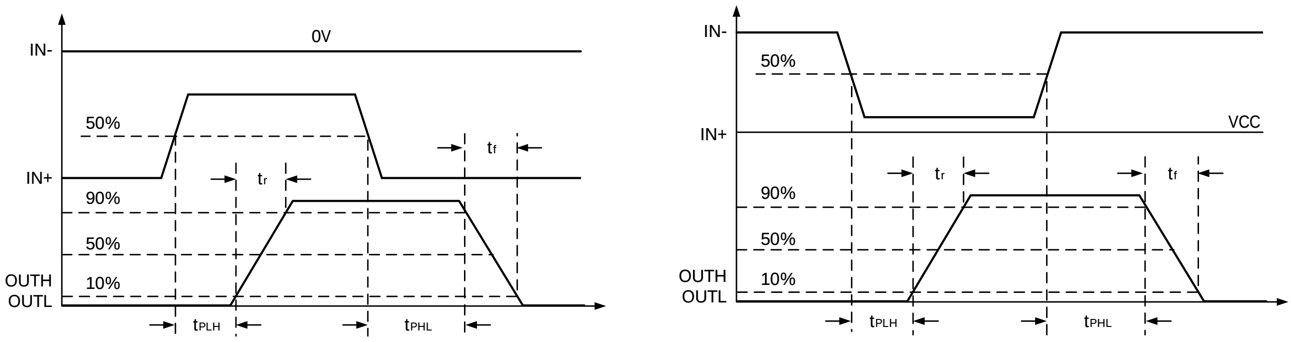


Figure 1. Input and Output Propagation Delay

8.2 CMTI

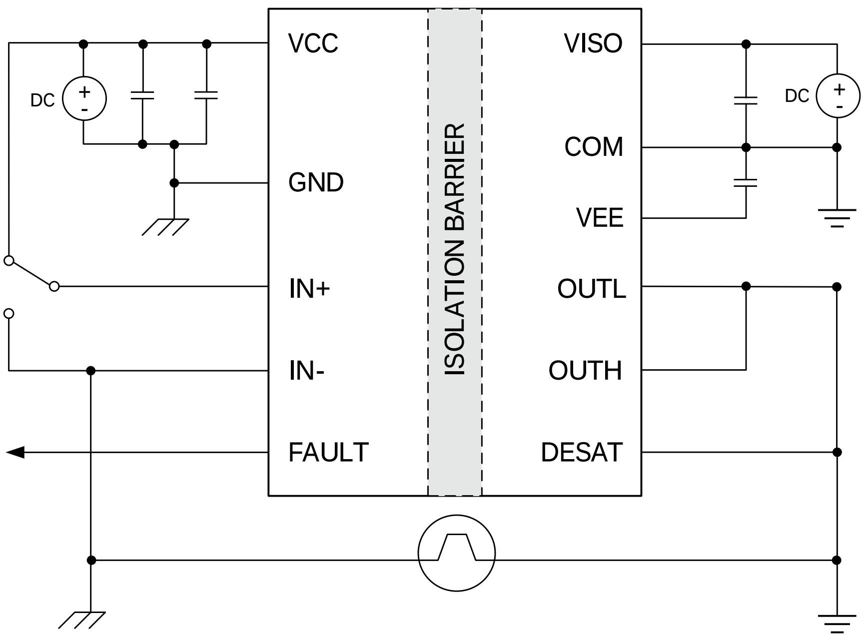


Figure 2. Simplified configuration of CMTI test

9.Function Description

9.1 Input Characteristic

The BTD3011x input pins are completely galvanic isolated from the secondary side. It adopts TTL level compatible design and supports 3.3V and 5V level inputs, which makes the chip easy to be controlled by a variety of micro controllers. Internal filtering circuit and input signal high/low level hysteresis are provided to improve the interference-immunity. The logic input pin IN+ has internal pull-down and IN- has internal pull-up, which ensures that the output pin OUTH is in a high impedance and OUTL is low when the chip is powered on, preventing the power devices from malfunctioning.

9.2 Drive Output Characteristic

The BTD3011x output stage utilizes rail-to-rail output. Both the high side and low side switches use NMOS for high current output capability. In order to drive the high side NMOS, bootstrap power supply is used. It is necessary to connect a capacitor CGXX between the OUTH pin and the VGXX pin.

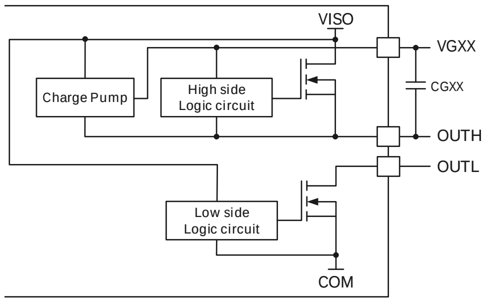


Figure 3. Dual NMOS drive output

9.3 Secondary Side Voltage Regulator

BTD3011x integrates a voltage regulator for secondary side supply internally, and automatically assigns positive and negative voltages according to the full voltage (VISO-COM) which is provided externally.

1) VISO-COM ⩽ 14V: The voltage is assigned to both positive and negative supply to ensure that the IGBT gate have negative drive voltage available during power on.

2) 14V < VISO-COM ⩽ 17V: The positive supply voltage at is kept 11.3V and the excess voltage is assigned to the negative supply.

3) 17V< VISO-COM ⩽ 21V: The negative supply voltage is kept at 5.3V and the excess voltage is assigned to the positive supply.

4) 21V <VISO-COM: The positive voltage is maintained at 15V, the excess voltage is assigned to the negative supply.

If the source or sink current of the VEE pin exceeds the limitation 3mA, VEE transits to constant current output mode and the voltage regulation is lost. Please avoid overload.

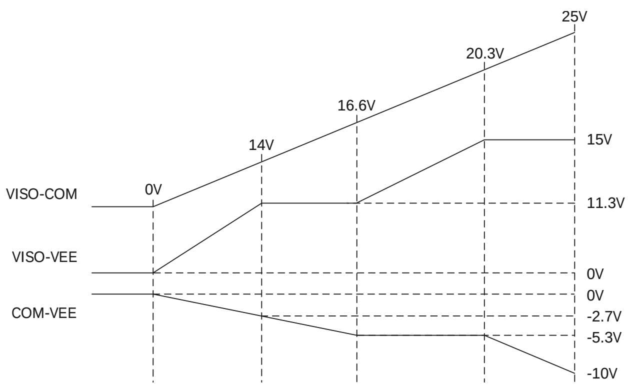


Figure 4. Voltage regulation characteristic

9.4 Undervoltage Lock Out Protection

The primary-side power supply, the secondary-side positive and negative power supply of the BTD3011x have an undervoltage lockout (UVLO) protection to prevent the occurrence of insufficient gate drive voltage. When the power supply voltage falls below the protection threshold, the driver IC will turn off the output to protect the power semiconductor device. When the power supply voltage returns to the recovery threshold, it resumes the output. To prevent repeated actions near the protection threshold, a hysteresis is applied. In order to avoid undetermined output state after power-on, the chip will first enter the undervoltage protection state, with the output pin OUTH in high-impedance state and OUTL in low-level until the power supply voltage is completely established and then start working.

9.5 Short Circuit Protection and Soft Shut Down

BTD3011x's secondary side integrates desaturation short-circuit protection. When there is a short-circuit current flowing through the CE/DS terminals of the IGBT/MOSFET during the turn-on transient, the forward voltage rises steeply, resulting in a sharp increase in the instantaneous power consumption of the IGBT/MOSFET and overheating damage to the IGBT/MOSFET. The voltage between CE/DS can be detected by the DESAT pin. When the voltage at the DESAT pin exceeds the fault threshold voltage, the driver output pin immediately shuts down the power device by means of soft shutdown (SSD), the FAULT pin is pulled down to GND to assert a fault. When the power device is turned off, the MOSFET Q_{CE} is turned on so that DESAT is shorted to COM to ensure that short-circuit protection will not be triggered. When the power device is turned on, Q_{CE} is turned off.
As the short circuit current is much higher than that during normal operation, to shut it down, a large di/dt can be generated, resulting in a high voltage spike. To effectively avoid the voltage spike, the driver activates a specific circuit after a short-circuit is detected, which samples and compares the gate voltage to a pre-configured soft transient reference, so that the device is shut down in a soft way.

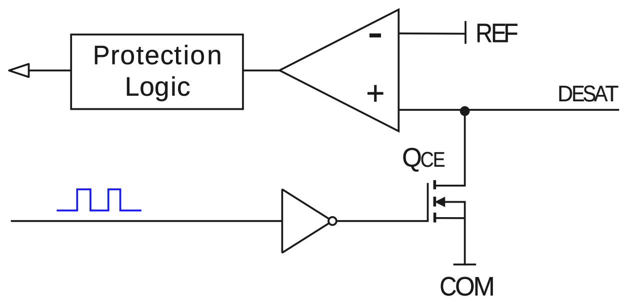


Figure 5. Short circuit protection circuit

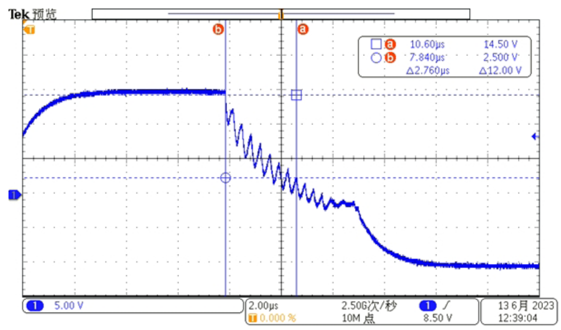


Figure 6. Experimental waveform of soft shut down

9.4 Input and Output Logic Table

IN+	IN-	OUTH	OUTL
H	L	H	Hi-Z
H	H	Hi-Z	L
L	L	Hi-Z	L
L	H	Hi-Z	L
Hi-Z：High impedance			

10.Applications

The following sections introduce the basic typical application of Bronze Technologies driver ICs, which is for reference only. In practical application, users need to verify and test its applicability according to their own design requirements to confirm the system functions.

10.1 Input and FAULT Pins

Depending on the input voltage level of the input, a resistor divider can be used. When 5V logic PWM signal is used as input, it is recommended that R1=100Ω and R2=47kΩ. In order to improve the immunity to high-frequency interference, it is recommended that a filtering capacitor CF=100pF be connected to GND, the effects of high-frequency interference and delay should be taken into consideration in selecting this parameter. The FAULT pin adopts open drain output, it is necessary to connect a pull-up resistor R_{SO} to the power supply VCC, it is recommended that R_{SO}=4.7kΩ.

10.2 Power Supply Pins

In order to ensure the stability of power supply, it is recommended to add suitable block capacitors between power supply pin and ground: capacitors C1=4.7uF and C2=470nF in parallel between the primary power supply VCC-GND, two capacitors C_{S21}=C_{S22}=4.7µF in parallel between the secondary power supply VISO-VEE, two capacitors C_{S21}=C_{S22}=4.7uF in parallel between the secondary power supply VEE-COM. Typically the capacitance of C_{S21}+C_{S22} and C_{S21}+ C_{S22} should be at least 3µF corresponds to 1uC total gate charge (QGATE). A charge pump circuit is integrated on the secondary side, a bootstrap capacitor needs to be connected between VGxx to OUTH with CGXX=10nF .

10.3 Drive Output Pins

The gate of the power device is connected to the OUTH pin via the turn-on resistor R_{GON} and to the OUTL pin via the turn-off resistor R_{GOFF}. In any case, the power consumption and temperature of the gate resistor need to be taken into account properly.

To ensure a stable gate voltage and to limit the collector or drain current during a short circuit, the gate is connected to the VISO pin via a Schottky diode D_{STO} (e.g. PMEG4010).

To avoid false conduction of the power devices during system power-up, a pull-down resistor R_{DIS} = 10 kΩ can be connected between the gate and the COM pin.

10.4 DESAT Pin

DESAT short-circuit protection can be achieved using either diode or resistor string. Figure 7 shows the use of diodes D_{VCE1} and D_{VCE2} for power device short-circuit desaturation detection. To ensure electrical insulation, two SMD package diodes (e.g., STTH212U) are typically used. the DESAT pin is connected to the VISO pin via resistor R_{RES}. When the power device is on, the current from the power supply VISO flows through RRES, the diodes and the power device into the VEE pin. At power device short-circuit desaturation, the diodes switch off and VISO charges C_{RES} through R_{RES}. In this configuration, the short circuit response time is determined by R_{RES} and C_{RES}. C_{RES}=33~330pF and R_{RES}=24~62kΩ are typically selected. Both CRES and R_{RES} can be adjusted if the desaturation is too sensitive or the short circuit duration is too long.

Figure 8 uses resistors R_{VCE2}-R_{VCE11} to detect short-circuit desaturation of power devices, the resistor value of R_{VCE2}-R_{VCE11} should be selected so that the current flowing through the resistor is limited to between 0.6mA and 0.8mA under the maximum DC bus voltage. E.g. the total resistance value of R_{VCE2}-R_{VCE11} should be approximately 1M for a 1200 V power device, with all resistors having a value of 100kΩ and in a 1206 package. In each case, the resistor string need to ensure sufficiently wide creepage distances and electrical clearances. Low leakage current diodes D_{CL} (e.g., BAS416) can keep the short-circuit response time stable over a wide range of DC bus voltages. The response time can be set by R_{VCE} and C_{RES} (typical values are 120kΩ and 33pF for 1200V devices, respectively). C_{RES} can be increased if short circuit detection is too sensitive. The maximum short circuit duration must be limited to the maximum value specified in the device datasheet.

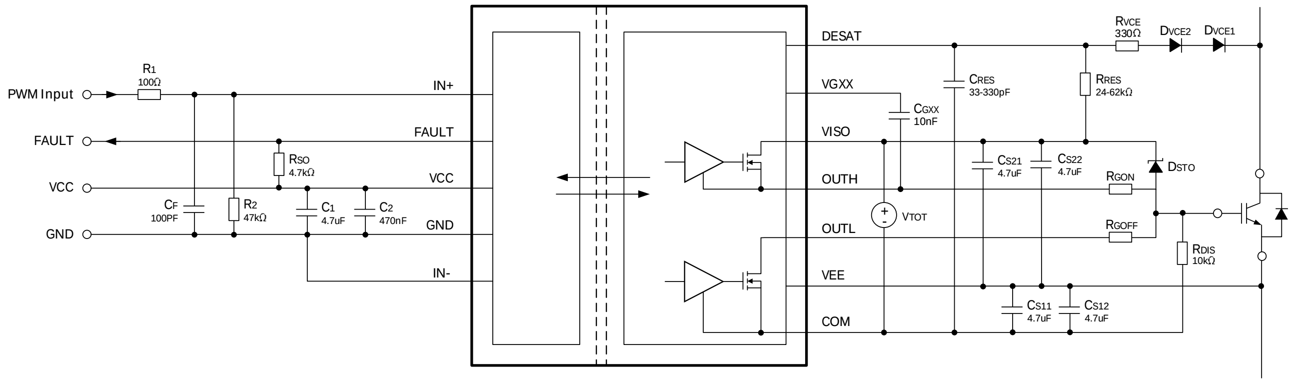


Figure 7. VCE detection using diode

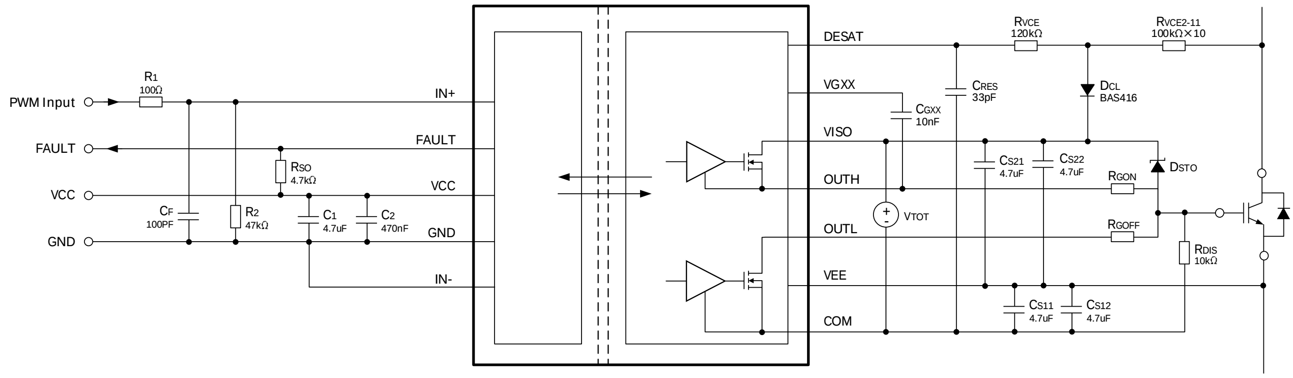
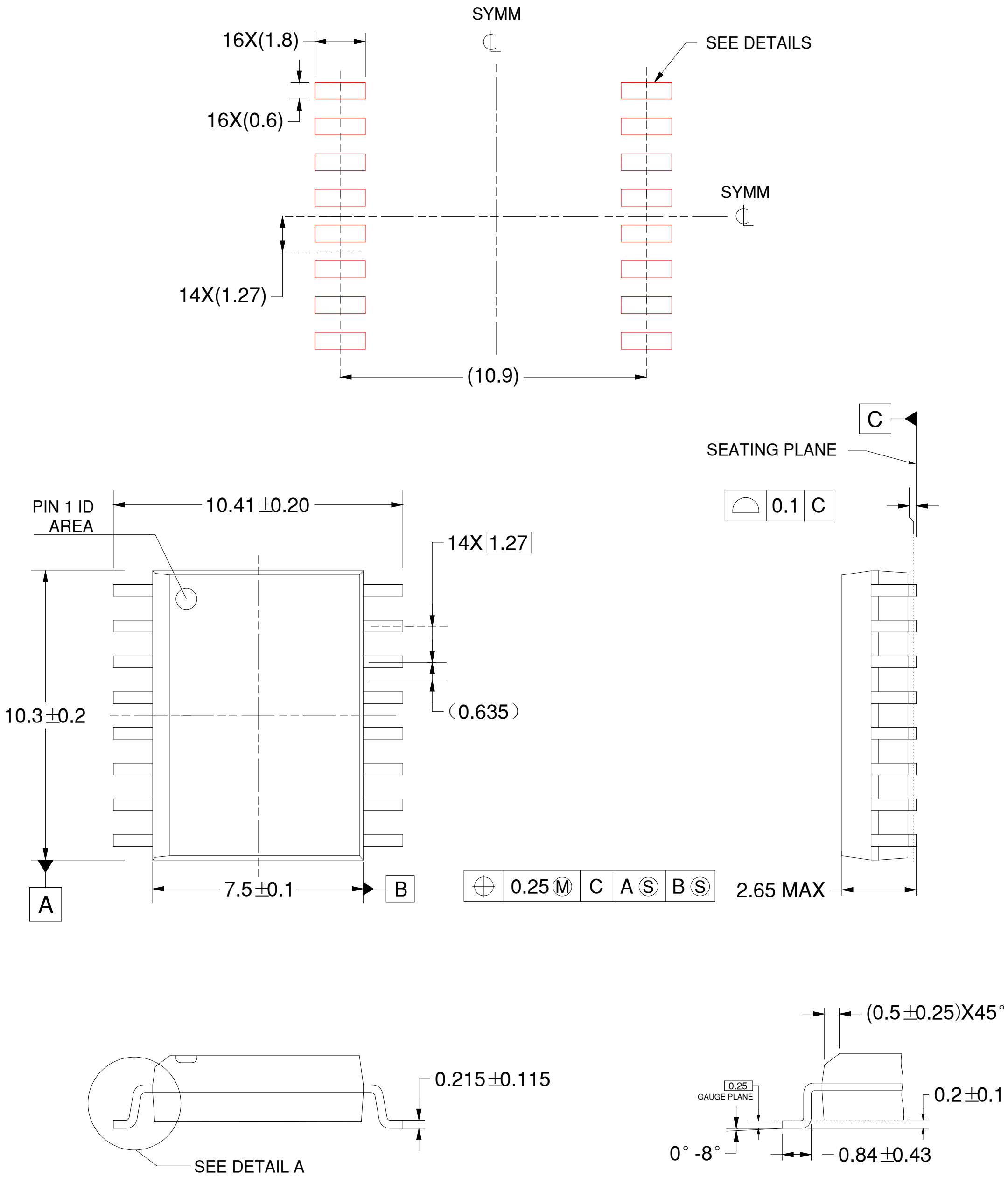


Figure 8. VCE detection using resistor string

11.Packaging and Packing Information

11.1 Package Identifier



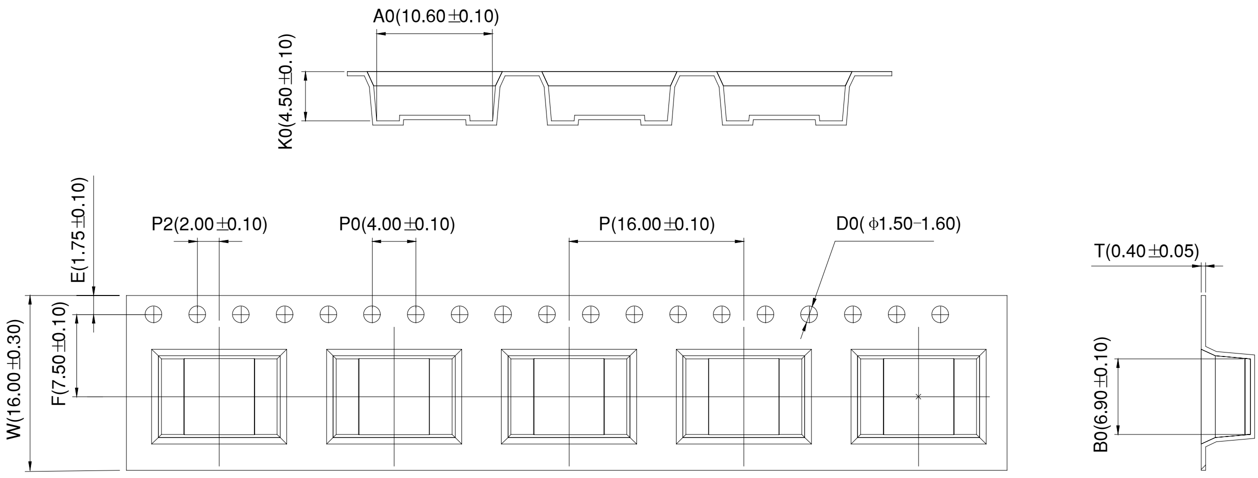
Note: 1) Legend unit: mm.

Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Bronze Technologies recommends that all integrated circuits be handled with appropriate precautions.Failure to observe proper handling and installation procedures can cause damage.

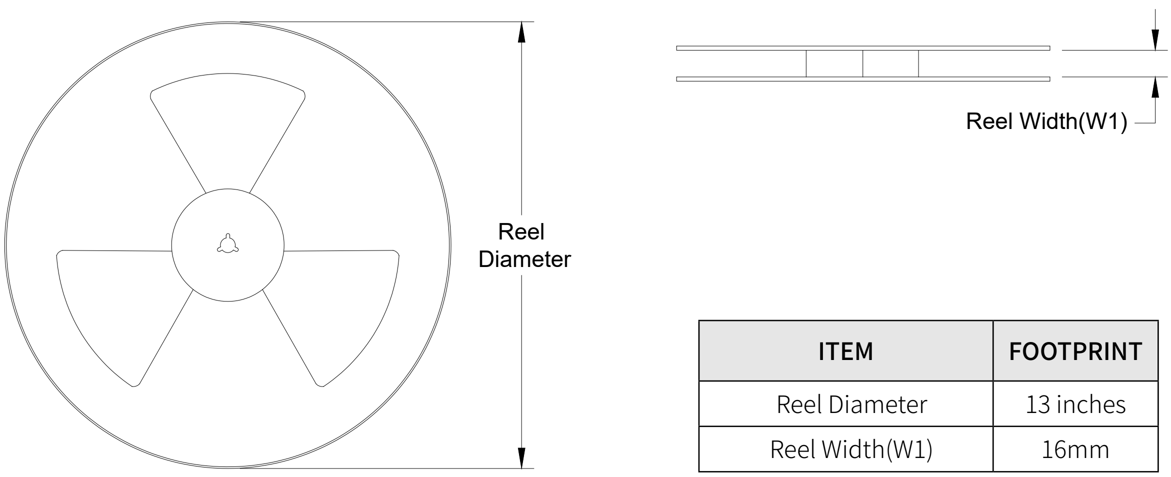
ESD damage can range from subtle performance degradation to complete device failure.Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.2 Packing Information



Note: 1) Legend unit: mm.

REEL DIMENSIONS



ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	16mm

12.Version Description

REVISION	NOTES	DATE
Rev.0.0	Released datasheet	05-Apr-2023
Rev.0.1	Content optimisation	07-Jun-2024

Bronze Technology Group | Shenzhen bronze Technology Co., Ltd

www.qtjtec.com
+86 0755 33379866
support@qtjtec.com