BTD21520x

Dual-Channel Isolated Gate Driver

1.Features

- Isolation voltage up to 5000Vrms(SOW-14)@UL1577; 3000Vrms(SOP-16)@UL1577
- Secondary-side drive voltage range up to 33V
- 4-A peak source, 6-A peak sink at output
- Integrated disable function
- Integrated dead time setting
- Typical propagation delay 45ns
- Operating temperature -40~125°C

2.Applications

Industrial:

- Power distribution
- Motor drives
- Isolated switched-mode power supplies
- Lighting systems
- Plasma displays
- PV and industrial inverters

Automotive:

- On-board chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid electric vehicles
- Battery electric vehicles

3.Description

BTD21520 is an isolated dual-channel gate driver with peak 4-A source current and peak 6-A sink current.It isolates primary-side from secondary-side by a 5k Vrms reinforced isolation barrier.

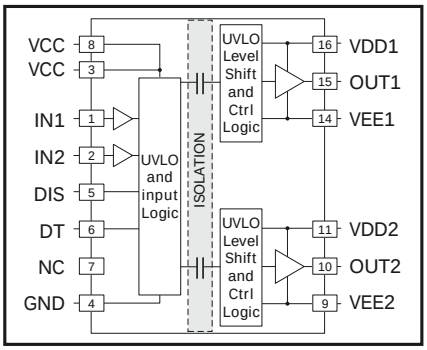
Internal functional isolation between the two secondary-side output channels allows a operating voltage of up to 1850 V_{DC}. The driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). Certain models include disable (DIS) pin. When the DIS pin is set high, it shuts down both outputs simultaneously. When the DIS pin is left open or grounded, it allows the device to operate normally.

RoHS COMPLIANT

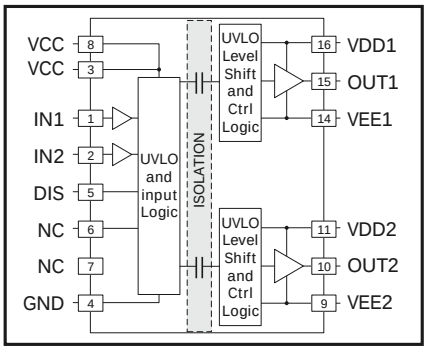
SOW-14

SOP-16

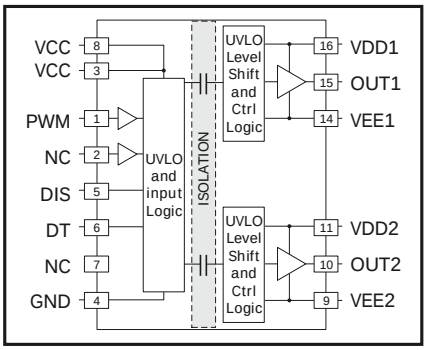
4.Functional Block Diagram



BTD21520M



BTD21520S



BTD21520E

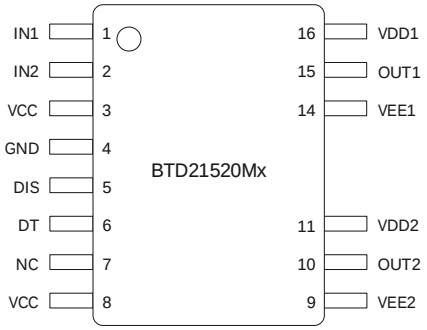
INDEX

5.Product Information

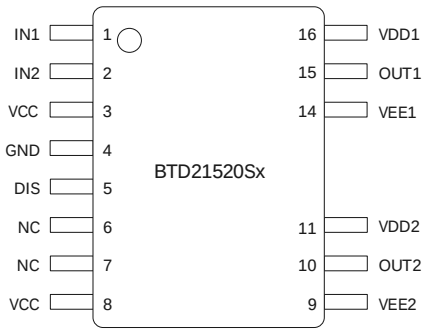
Part No.	Pin Configuration	Secondary Side UVLO Threshold	Operating Temperature	Package	Package Material	Quantity	Marking
BTD21520MAWR	Dual-channel non-inverting input, dead time configuration and disable function	6V	-40-125°C	SOW-14	Tape & Reel	1500pcs /Reel	BTD21520MA
BTD21520MBWR		8V					BTD21520MB
BTD21520SAWR	Dual-channel non-inverting input, disable function	6V					BTD21520SA
BTD21520SBWR		8V					BTD21520SB
BTD21520EAWR	Single PWM input, dead time configuration and disable function	6V					BTD21520EA
BTD21520EBWR		8V					BTD21520EB
BTD21520MAPR	Dual-channel non-inverting input, dead time configu-rtion and disable function	6V	-40-125°C	SOP-16	Tape & Reel	2500pcs /Reel	BTD21520MA
BTD21520MBPR		8V					BTD21520MB
BTD21520SAPR	Dual-channel non-inverting input, disable function	6V					BTD21520SA
BTD21520SBPR		8V					BTD21520SB
BTD21520EAPR	Single PWM input, dead time configuration and disable function	6V					BTD21520EA
BTD21520EBPR		8V					BTD21520EB

6.Pin Configuration and Functions

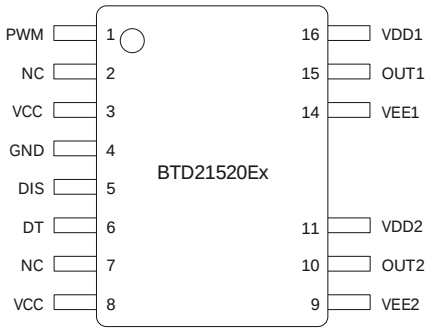
6.1 BTD21520Mx

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	IN1	I	Input signal for channel 1	
2	IN2	I	Input signal for channel 2	
3	VCC	P	Primary-side supply voltage	
4	GND	G	Primary-side ground reference	
5	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
6	DT	I	Programmable dead time function	
7	NC	-	No Internal connection	
8	VCC	P	Primary-side supply voltage	
9	VEE2	P	Ground for secondary-side driver 2	
10	OUT2	O	Output of driver 2	
11	VDD2	P	Secondary-side power for driver 2	
14	VEE1	P	Ground for secondary-side driver 1	
15	OUT1	O	Output of driver 1	
16	VDD1	P	Secondary-side power for driver 1	
(1) P=Power, G=Ground, I=Input, O=Output				

6.2 BTD21520Sx

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	IN1	I	Input signal for channel 1	
2	IN2	I	Input signal for channel 2	
3	VCC	P	Primary-side supply voltage	
4	GND	G	Primary-side ground reference	
5	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
6	NC	-	No Internal connection	
7	NC	-	No Internal connection	
8	VCC	P	Primary-side supply voltage	
9	VEE2	P	Ground for secondary-side driver 2	
10	OUT2	O	Output of driver 2	
11	VDD2	P	Secondary-side power for driver 2	
14	VEE1	P	Ground for secondary-side driver 1	
15	OUT1	O	Output of driver 1	
16	VDD1	P	Secondary-side power for driver 1	
(1) P=Power, G=Ground, I=Input, O=Output				

6.3 BTD21520Ex

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	PWM	I	PWM control signal input	
2	NC	-	No Internal connection	
3	VCC	P	Primary-side supply voltage	
4	GND	G	Primary-side ground reference	
5	DIS	I	Disables both driver outputs if asserted high, enables if set low or left open	
6	DT	I	Programmable dead time function	
7	NC	-	No Internal connection	
8	VCC	P	Primary-side supply voltage	
9	VEE2	P	Ground for secondary-side driver 2	
10	OUT2	O	Output of driver 2	
11	VDD2	P	Secondary-side power for driver 2	
14	VEE1	P	Ground for secondary-side driver 1	
15	OUT1	O	Output of driver 1	
16	VDD1	P	Secondary-side power for driver 1	

(1) P=Power, G=Ground, I=Input, O=Output

7.Specification Parameters

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Input bias pin supply voltage (pin 3/pin 8)	GND-0.3	GND+6.5	V
VDDx	Driver bias supply (to VEEx)	VEEx-0.3	VEEx+35	
V_O	Output signal voltage	VEEx-0.3	VDDx+0.3	
V_{IN}	Input signal voltage (INx, PWM, DIS, DT to GND)	GND-0.3	VCC+0.3	
-	Channel to channel voltage	-	1850	
T_J	Operating Junction Temperature	-40	150	°C
T_S	Storage Temperature	-65	150	
T_L	Soldering Temperature (10s)	-	300	
ESD	Human-body model (HBM)	±4000		V
	Charge-device model (CDM)	±1500		
-	Input signal voltage(IN1,IN2 Transient for 50ns)	-5	VCC+0.3	
Note: The above are stress levels only.Devices are not recommended to operate under these or any other conditions beyond these values.Prolonged operation under the absolute maximum rating may affect the reliability of the device, and in severe cases it may cause permanent damage to the devices.				

7.2 Thermal Information

SYMBOL	DESCRIPTION	SOW-14	SOP-16	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.6	41.2	°C /W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.5	7.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	24.9	
ψ_{JT}	Junction-to-top characterization parameter	31.5	10.9	
ψ_{JB}	Junction-to-board characterization parameter	41.7	29.2	

7.3 Power Ratings

SYMBOL	PARAMETER	TEST CONDITIONS	SOW-14	SOP-16	UNIT
P_D	Power dissipation by BTD21520x	VCC=5V, VDD1/2=12V, IN1/2=3.3V, 3MHz, 50% duty cycle square wave, 1nF load	1.103	1.102	W
P_{D1}	Power dissipation by each driver side of BTD21520x		0.531	0.533	
P_{D2}			0.561	0.558	
P_{DI}	Power dissipation by transmitter side of BTD21520x		0.011	0.011	

7.4 Recommended Operation Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VCC	Input supply voltage	-	3	5	V
VDDx	Driver output bias supply	-	-	33	
V_{IN}	Input voltage range IN1, IN2, PWM	-	0	VCC	
T_A	Operating ambient temperature	-	-40	125	°C

7.5 Safety-Limiting Values

SYMBOL	PARAMETER	TEST CONDITIONS		SIDE	MIN	MAX	UNIT
I_S	Safety output supply current	T_A=25°C , T_J= 150°C	VDD1/2=12V	OUT1, OUT2	-	75	mA
			VDD1/2=25V	OUT1, OUT2	-	36	
P_S	Safety supply power	VDD1/2=25V, T_A=25°C , T_J=150°C		INPUT	-	50	mW
				OUT1	-	900	
				OUT2	-	900	
				TOTAL	-	1850	
T_S	Safety temperature (1)				-	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

7.6 Electrical Characteristics

T_A=-40~125°C , VCC=3.3 or 5V, VDD1=VDD2=12V, C_L (1) =100pF.Output pin: current towards outside of the chip is positive direction; Input pin: current towards inside of the chip is positive direction.

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Characteristics							
V_{IH}	Input logic 1 (INx, DIS, PWM)		VCC=5V	2.1	2.4	2.7	V
V_{IL}	Input logic 0 (INx, DIS, PWM)		-	1.1	1.4	1.7	
V_{IN_HYS}	Input Hysteresis		-	-	1	-	
I_{VCC}	VCC quiescent current		-	-	1.5	2	mA
I_{VDDx}	VDDx quiescent current		-	-	1	1.8	
Primary side UVLO Thresholds (VCC)							
V_{ON1}	Rising threshold		-	-	2.6	-	V
V_{OFF1}	Falling threshold		-	-	2.5	-	
$V_{UV,HYS1}$	Threshold hysteresis		-	-	0.1	-	
Secondary side UVLO Thresholds (VDDx)							
V_{ON2}	Rising threshold	BTD21520xAx	-	-	6	6.3	V
V_{OFF2}	Falling threshold		-	5.4	5.7	-	
$V_{UV,HYS2}$	Threshold hysteresis		-	-	0.3	-	
V_{ON2}	Rising threshold	BTD21520xBx	-	-	8.7	9.2	
V_{OFF2}	Falling threshold		-	7.8	8.2	-	
$V_{UV,HYS2}$	Threshold hysteresis		-	-	0.5	-	
Output Characteristics							
I_{OH}	Peak output source current		C_{VDD}=10μF, C_{LOAD}=0.18μF, f=1kHz	-	4	-	A
I_{OL}	Peak output sink current			-	6	-	
I_{VTS}	OUTx pin reverse sinking tolerance		1us pulse	-	5	-	
VDD-V_O	Output voltage at high state		I_{OUT}=10mA	-	60	-	mV
V_O-VEE	Output voltage at low state		I_{OUT}=-10mA	-	5.5	-	
R_{OHx}	Output resistance at high state		I_{OUT}=10mA, T_A=25°C	-	6.5	-	Ω
R_{OLx}	Output resistance at low state		I_{OUT}=-10mA, T_A=25°C	-	0.5	-	
Active Pull-Down Function							
V_{OUTSD}	Active pull-down function, the voltage value of OUTx pin to VEEx pin in event of loss of power on VDDx		I_{OUT}=-1A, VDDx=floating	-	2.5	-	V

(Continued)

Switching Parameters							
t_{PLH}	Propagation delay from INx to OUTx rising edges		-	-	40	-	ns
t_{PHL}	Propagation delay from INx to OUTx falling edges		-	-	45	-	
t_r	Output rise time		C_L=1nF, 20% to 80%	-	10	26	ns
t_f	Output fall time		C_L=1nF, 90% to 10%	-	10	26	
t_{PWD}	Pulse width distortion $\lvert t_{PHL}-t_{PLH}\rvert$		-	-	-	10	
t_{DM}	Propagation delays matching between VOUT1, VOUT2		f=100kHz, IN1=IN2	-	-	5	
DT	Dead time		DT pull up to VCC	Two output channels are completely independent			-
			DT pin open (not recommended)	-	8	15	ns
			R_{DT}=20kΩ	160	200	250	
t_{sk}	Delay variation between samples		Under the same supply voltage, operating temperature, input and load conditions, C_L=100pF	-	1	25	ns
-	Undervoltage lockout recovery time	$t_{VCC+ \text{ to OUT}}$	-	-	40	-	µs
		$t_{VDD+ \text{ to OUT}}$	-	-	50	-	
CMTI	Common-mode transient immunity		INx tied to GND or VCC, V_{CM}=1500V	100	-	-	kV/µs
(1) C_L: Load capacitance from output pin OUTx to VEEx.							

7.7 SAFETY PARAMETERS

7.7.1 WIDE-BODY PACKAGE (SOW-14)

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLR	External clearance	Shortest pin-to-pin distance through air	8.5	-	-	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	8.5	-	-	
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2×8.5 μm)	17	-	-	μm
CTI	Comparative tracking index	DIN EN 60112	600	-	-	V
-	Overvoltage category	Voltage rating < 600Vrms	I-III	-	-	-
		Voltage rating < 1000Vrms	I-II	-	-	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	-	-	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown	1500	-	-	Vrms
V_{IOTM}	Maximum transient isolation voltage	100% V_{IOTM}, 60s, 120% V_{IOTM}, 1s	7000	-	-	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	IEC 62368-1, 1.2/50us waveform, 1.6 x V_{IOSM}	8000	-	-	
Q_{pd}	Apparent charge	Method a, After Input/Output safety test subgroup 2/3.V_{IN}= V_{IOTM}, 60s, V_{pd}=1.2 V_{IOTM}, 10s	-	-	5	pC
		Method a, After environmental tests subgroup 1. V_{IN}=V_{IOTM}, 60s, V_{pd}=1.6V_{IOTM}, 10s	-	-	5	
		Method b1; At routine test (100% production) and preconditioning (type test) V_{IN}=1.2V_{IOTM}, 1s, V_{pd}=1.875V_{IOTM}, 1s	-	-	5	
C_{IO}	Barrier capacitance, input to output	V_{IO}=0.4V_{peak}, f=1MHz, sine wave	-	1.2	-	pF
R_{IO}	Isolation resistance, input to output	Test voltage of 500V, T_A=25°C	10^{12}	-	-	Ω
		Test voltage of 500V, 100°C< T_A < 125°C	10^{11}	-	-	
		Test voltage of 500V, T_A=150°C	10^9	-	-	
-	Pollution degree	-	-	2	-	-
V_{ISO}	Withstand isolation voltage	V_{TEST}=V_{ISO}=5000Vrms, t=60 sec(qualification), V_{TEST}=1.2×V_{ISO}=6000Vrms, t=1 sec(100% production)	5000	-	-	Vrms

7.7.2 Safety-Related Certifications (SOW-14)

UL	VDE	CQC
Recognized under UL 1577 Component Recognition Program	Plan to certify according to DIN V VDE V0884-11:2017-01 and DIN EN 61010-1	Plan to certify according to GB 4943.1-2011
Single protection, 5000 V_{RMS}	Reinforced Insulation Maximum Transient isolation Overvoltage, 7000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 2121 V_{PK}; Maximum Surge Isolation Voltage, 8000 V_{PK}	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate

8.Parameter Testing

8.1 Propagation Delay and Pulse Width Distortion

The figure below shows the characterization of pulse width distortion (t_{PWD}) and delay matching (t_{DM}). During the test, both inputs are in phase, the dead time function is disabled by shorting the DT Pin to VCC.

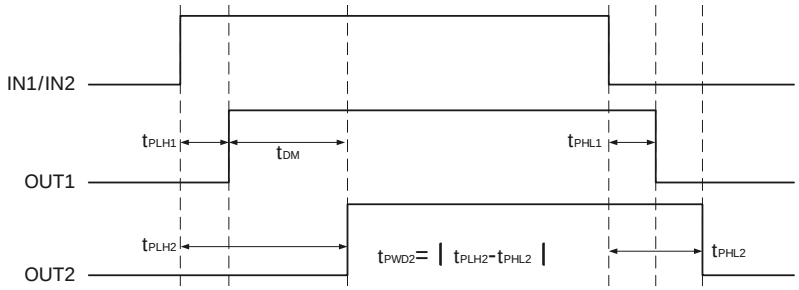


Figure 1. Dead Time Disabled, IN1 and IN2 with synchronized signal

8.2 Rise Time and Fall Time

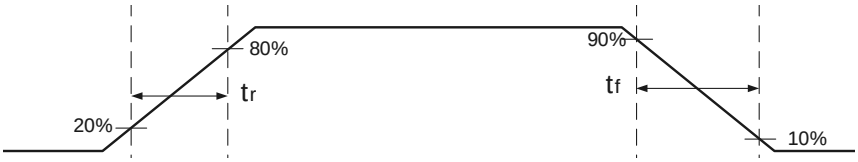


Figure 2. Definition of Rise Time and Fall Time

8.3 Input and Disable Response Time

When the DIS pin is connected to the controller at a certain distance, it is recommended to configure a bypass capacitor of about 1nF with low stray inductance close to the DIS pin.

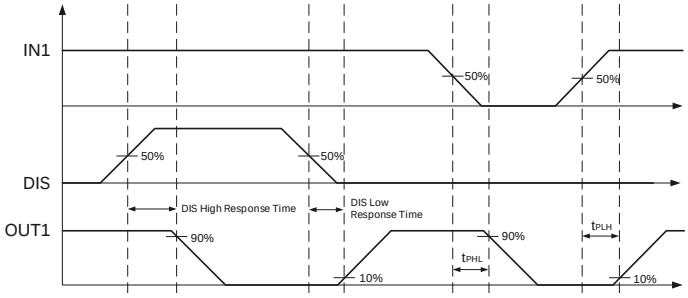


Figure 3. Disable Pin Timing

8.4 Programmable Dead Time

DT pin left open or connected to GND via resistor R_{DT} sets dead time between two channels.

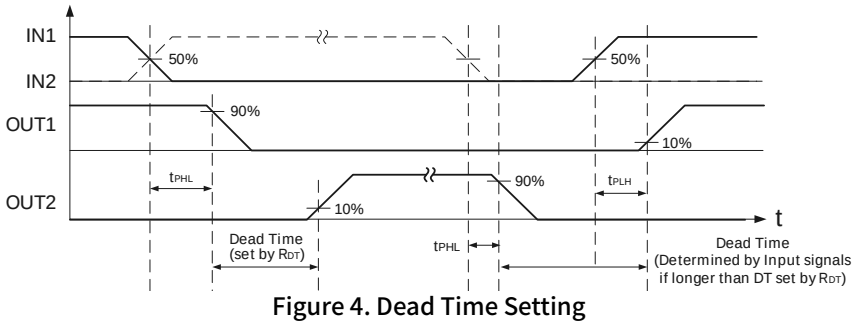


Figure 4. Dead Time Setting

8.5 CMTI Testing

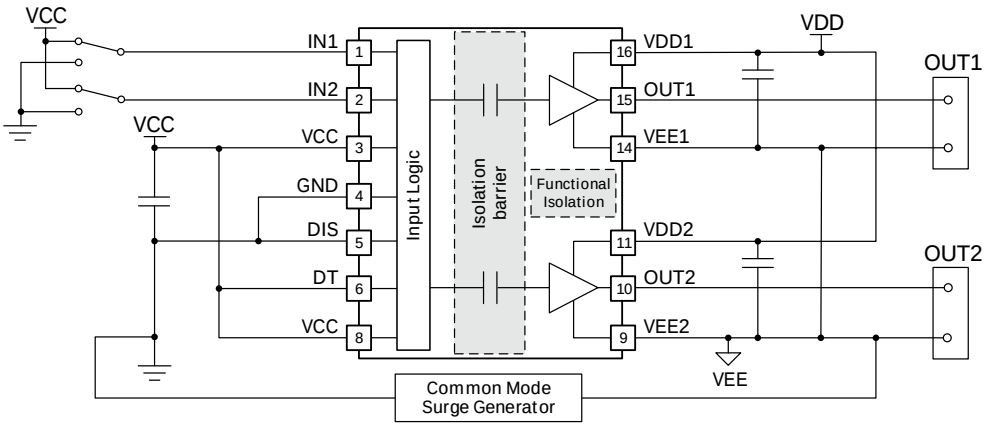


Figure 5. Simplified CMTI Test Setup

8.6 UVLO Delay During IC Power-On

At the process of device power-on, there is a time delay from the start of the supply voltage rise to the UVLO recovery threshold, and then to the device output response, as shown in the figures below. $t_{VCC+\ to\ OUT}$ is primary side power-on UVLO delay (typical value 40μs), and $t_{VDD+\ to\ OUT}$ is secondary side power-on UVLO delay (typical value 50us). It is suggested that after powering on the driver IC, adequate time margin is reserved before sending PWM signal to IC.

If IN1 or IN2 is already at high level before VCC or VDDx reaches the recovery threshold, after $t_{VCC+\ to\ OUT}$ or $t_{VDD+\ to\ OUT}$ counting from the time point when VCC or VDDx reaches the recovery threshold, the corresponding output will jump to a high level. However, when the VCC or VDDx voltage drops to the UVLO lockout threshold, the output will be completely blocked within 1us. This asymmetric design is to ensure safe operation of a VCC or VDDx in the event of a power failure.

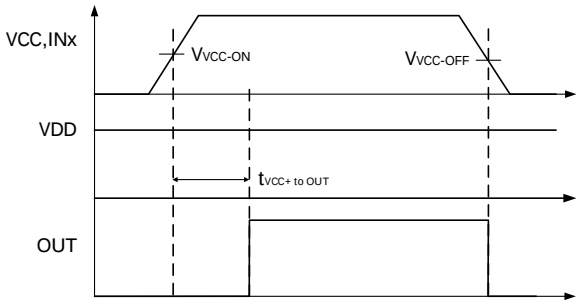


Figure 6. UVLO delay when the VCC is powered on

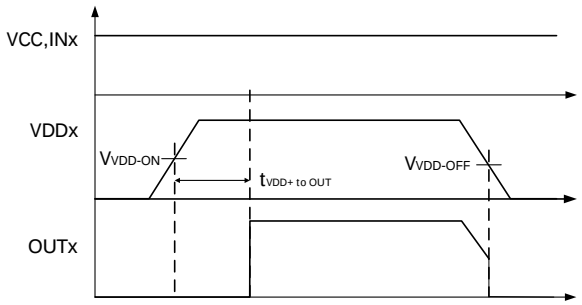


Figure 7. UVLO delay when the VDDx is powered on

8.7 Typical Characteristics

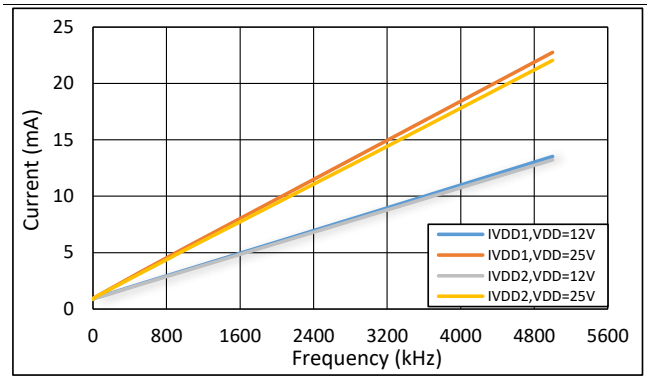


Figure 8. Secondary side per channel current consumption vs frequency
(No Load, VDDx = 12 V or 25 V)

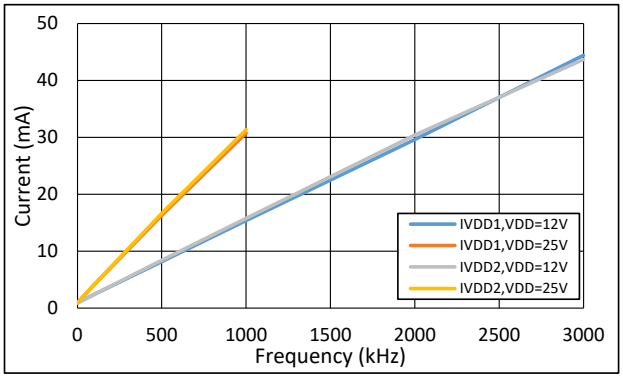


Figure 9. Secondary side per channel current consumption vs frequency
(1-nF Load, VDDx = 12 V or 25 V)

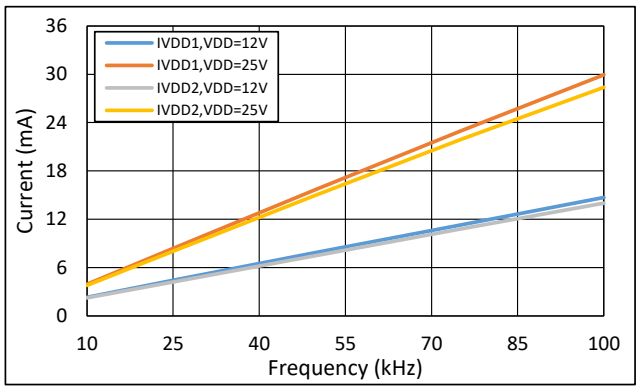


Figure 10. Secondary side per channel current consumption vs frequency
(10-nF Load, VDDx = 12 V or 25 V)

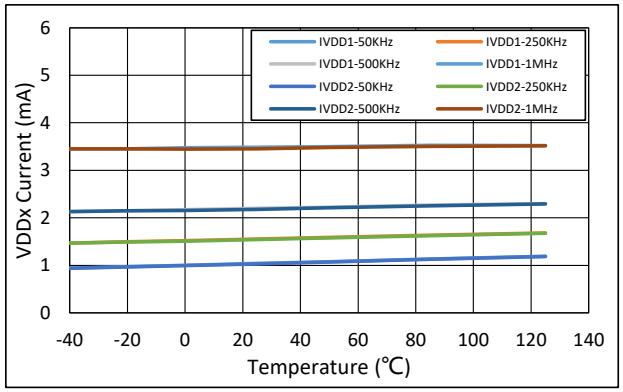


Figure 11. Secondary side per channel supply current Vs. temperature
(No load, Different switching frequencies)

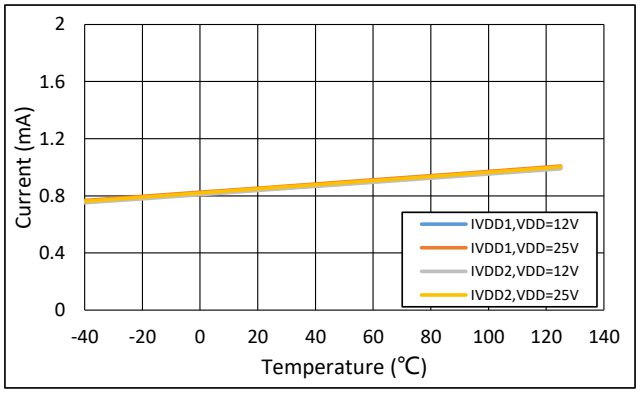


Figure 12. Secondary side per channel quiescent supply current vs temperature
(No load, input low, no switching)

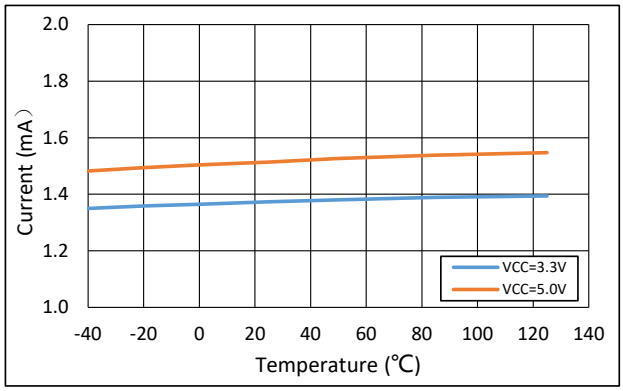


Figure 13. Primary side quiescent supply current vs temperature
(No load, input low, no switching)

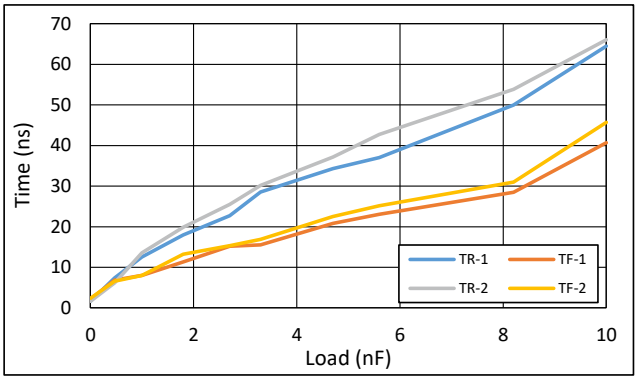


Figure 14. Rising and falling times vs load (VDDx = 12 V)

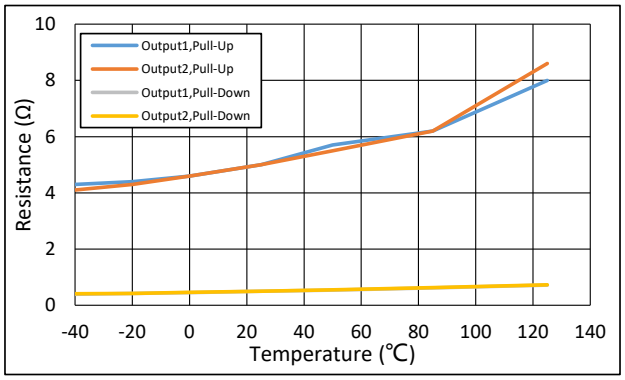


Figure 15. Output resistance vs temperature

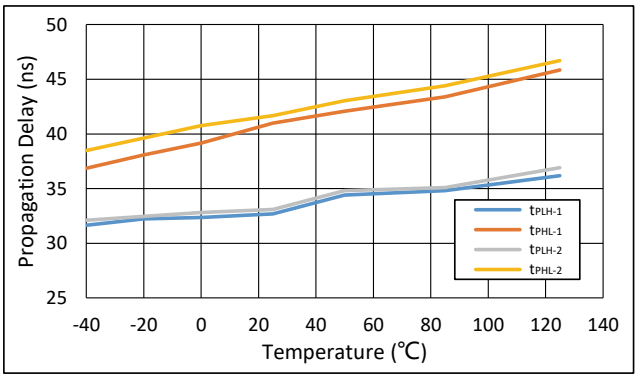


Figure 16. Propagation delay vs temperature

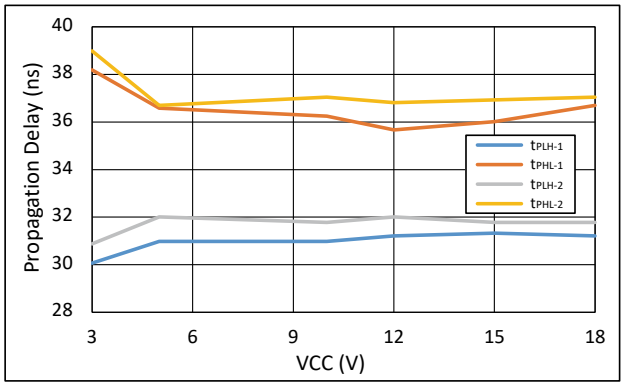


Figure 17. Propagation delay vs VCC

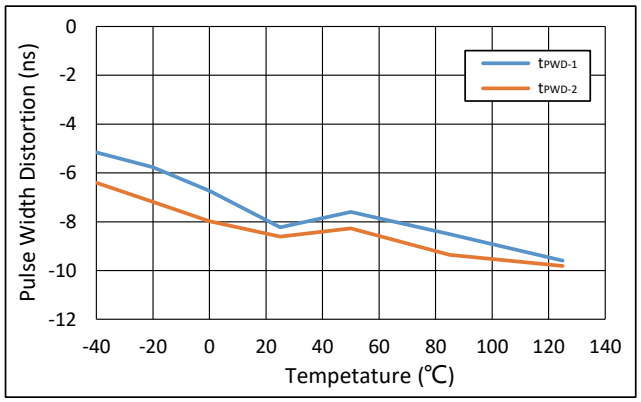


Figure 18. Pulse width distortion vs temperature

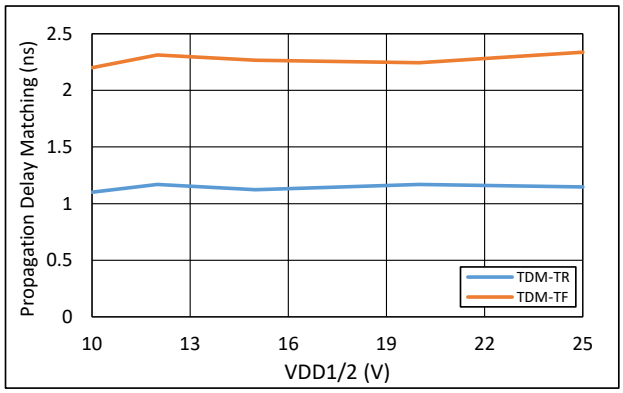


Figure 19. Propagation delay matching vs VDDx

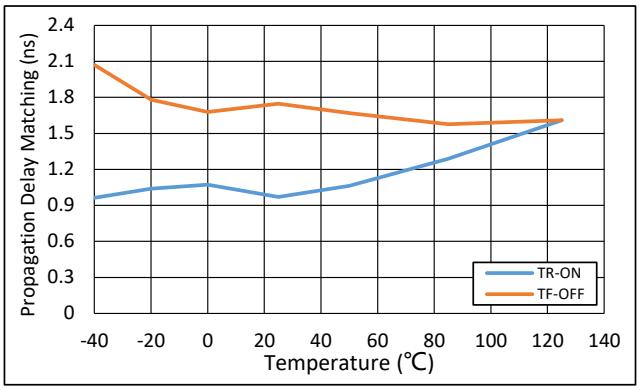


Figure 20. Propagation delay matching vs temperature

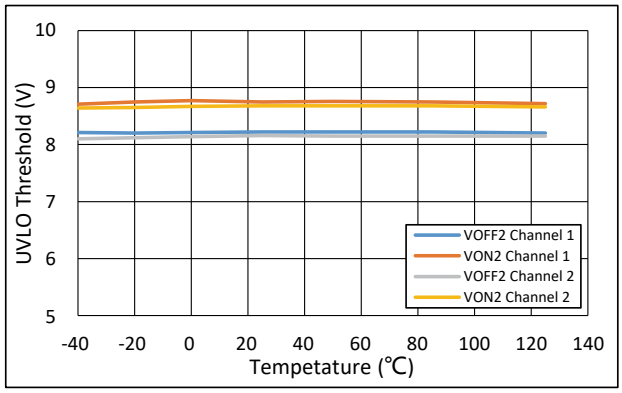


Figure 21. VDDx 8-V UVLO hysteresis vs temperature

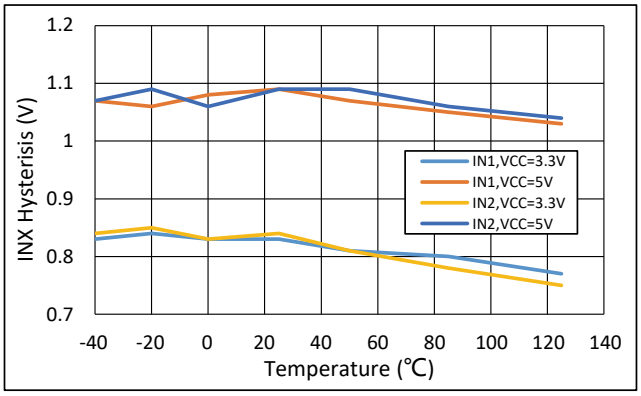


Figure 22. INx hysteresis vs temperature

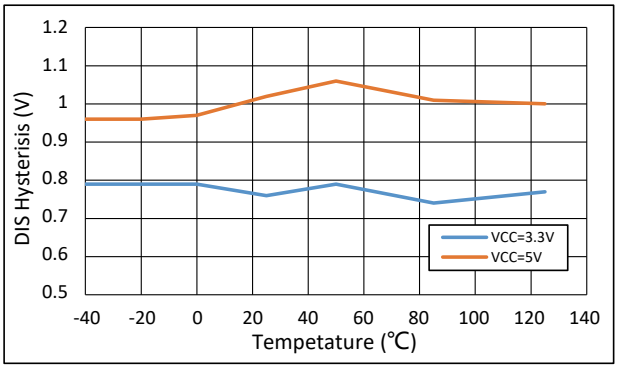


Figure 23. DIS hysteresis vs temperature

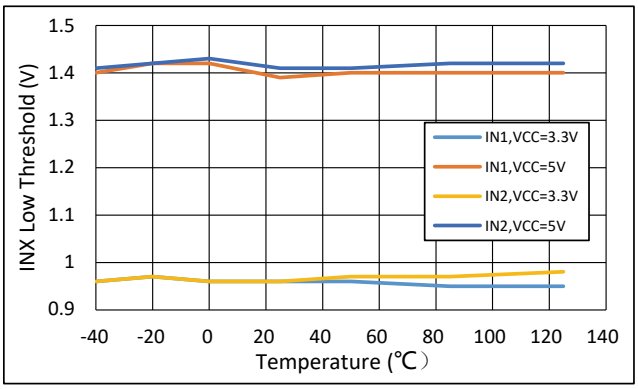


Figure 24. INx low threshold vs temperature

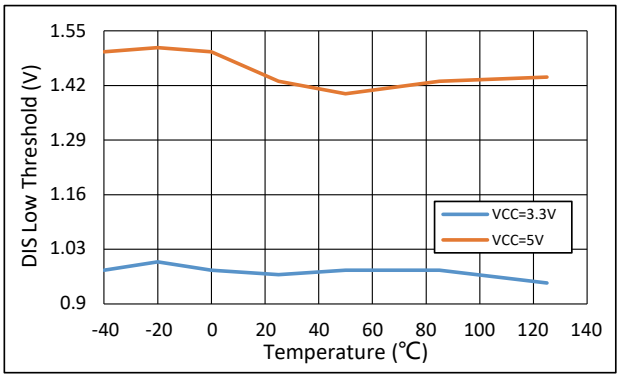


Figure 25. DIS low threshold vs temperature

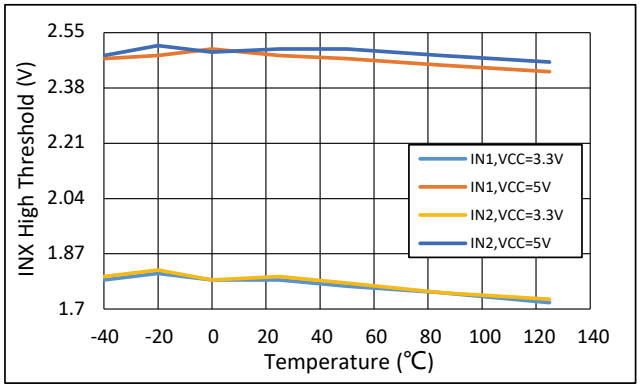


Figure 26. INx high threshold vs temperature

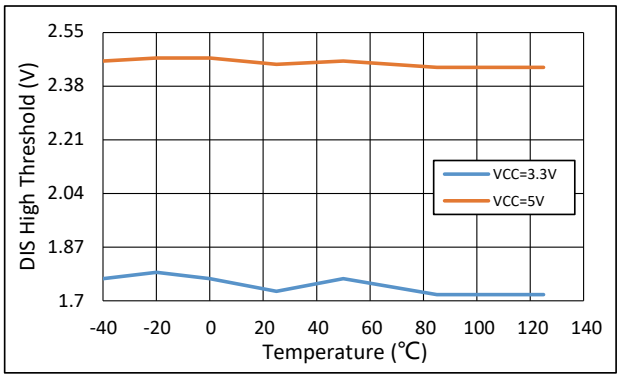


Figure 27. DIS high threshold vs temperature

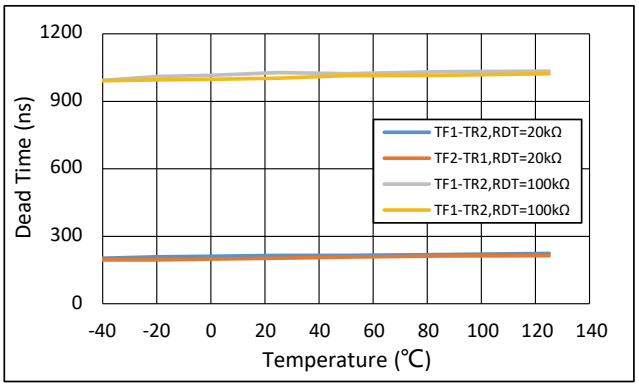


Figure 28. Dead time vs temperature

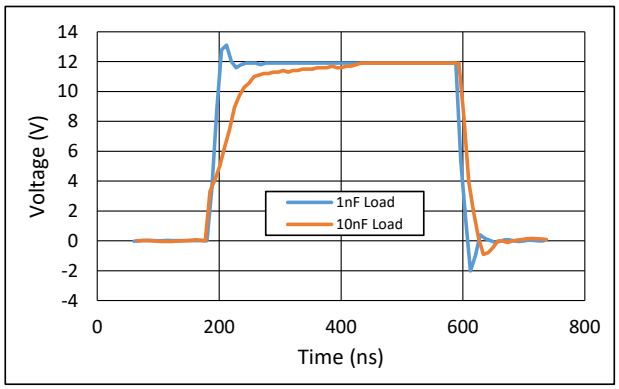


Figure 29. Typical output waveforms

9.Function Description

9.1 Block Diagram

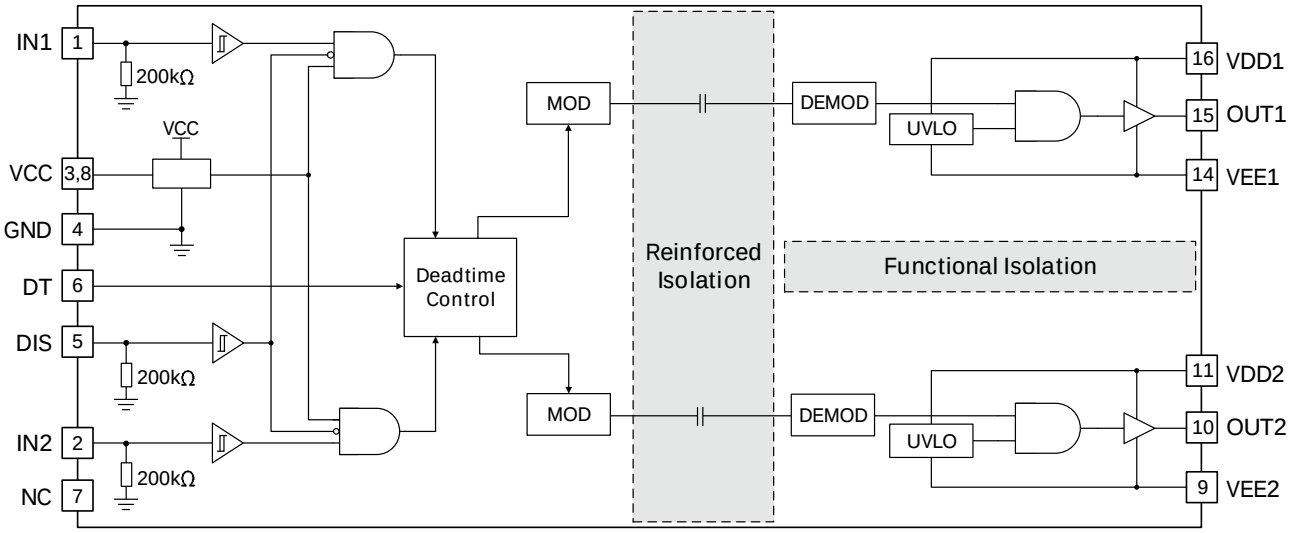


Figure 30. Functional Block Diagram (BTD21520Mx)

9.2 Input and Output Logic Table

When VCC and VDD are powered on, the relevant input and output logic information is as follows:

BTD21520M

INPUT		DIS	OUTPUT		DESCRIPTION
IN1	IN2		OUT1	OUT2	
L	L	L or left open	L	L	If dead time function is used, output switching occurs after the dead time ended.See Programmable Dead Time (DT) pin
L	H	L or left open	L	H	
H	L	L or left open	H	L	DT is left open or programmed with R_{DT}
H	H	L or left open	H	H	DT pin pulled to VCC
Left open	Left open	L or left open	L	L	-
X	X	H	L	L	-

BTD21520S

INPUT		DIS	OUTPUT		DESCRIPTION
IN1	IN2		OUT1	OUT2	
L	L	L or left open	L	L	No internal dead time setting, two output channels are independent
L	H	L or left open	L	H	
H	L	L or left open	H	L	
H	H	L or left open	H	H	
Left open	Left open	L or left open	L	L	-
X	X	H	L	L	-

BTD21520E

PWM INPUT	DIS	OUTPUT		DESCRIPTION
		OUT1	OUT2	
H	L	H	L	If dead time function is used, output jumps after dead time ended. See Programmable Dead Time (DT) pin
L/Left open	L	L	H	
X	H	L	L	Device disabled
(1) "X" means L, H or left open.				

9.3 Input Stage Characteristics

With input pins and secondary side completely isolated, BTD21520 is designed to be compatible with CMOS levels, and supports 3.3V, 5V and 15V level input, making the chip easy to accept control of multiple logic levels.Inputs with Schmitt stage for improved anti-interference performance.INx, PWM, and DIS have a built-in 200kΩ resistor pulled down to the ground, ensuring that the output of the device is low when the input is left open However, in order to ensure the initial power-on state of the device, it is recommended to add an appropriate pull-up or pull-down resistor to the input.

9.4 Output Booster Characteristic

The BTD21520 has a rail-to-rail booster stage output. The pull-up structure of the output stage consists of a P-channel MOSFET and an N-channel MOSFET connected in parallel. At turn-on, N-channel MOSFET provides high current driving capability. P-channel MOSFET provides a small steady-state conduction voltage drop. The PMOS on-resistance (R_{OH}) is 6.5Ω, and the NMOS on-resistance (R_{NMOS_ON}) is 0.5Ω.

The pull-down structure is implemented using an N-channel MOSFET. A 1MΩ resistor is connected in parallel between the drain and gate of the MOSFET to effectively clamp the gate voltage of the power device in the event of a loss of pow-er to prevent the occurrence of partial turn-on.However, in order to ensure reliable shutdown of the power device, it is recommended that appropriate pull-down resistor be added to the gate.

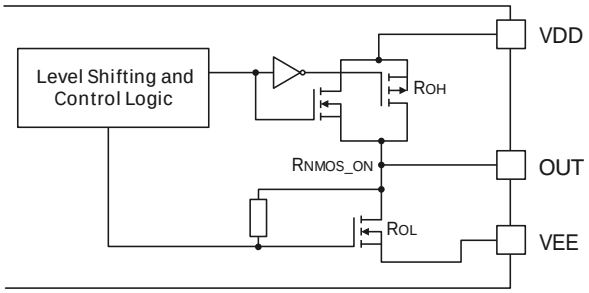


Figure 31.Output Characteristics Diagram

9.5 Device Function

9.5.1 Disable

When the DIS pin is set high, both outputs can be shut down at the same time. The device operates normally when the DIS pin is grounded or left open. The response time of the disable function is within 20ns. The disable function is activated or deactivated according to the input only when the VCC is kept above the undervoltage turn-on threshold. If the DIS pin is not used, it is recommended to connect it to the ground. If connecting DIS pin to a microcontroller with distance, it is recommended to bypass the DIS pin with a low ESR/ESL capacitor of approximately 1nF for better noise immunity.

9.5.2 Pulling DT Pin Up to VCC

The two channels are independent, with output exactly matching input, and no dead time is inserted, allowing the output signals to be both high.

9.5.3 Dead Time Setting

DT pin sets the dead time.It is used to set the dead time between channel 1 and channel 2 to prevent them from shoot-through. The steady-state voltage of DT pin is 0.8V, and the current value of the pin is measured for corresponding dead time. The dead time is calculated as $t_{DT}=10\times R_{DT}$. The unit of t_{DT} is ns and the unit of R_{DT} is kΩ. To ensure that the pin signal is not interfered, it is recommended to place a 2.2nF capacitor near the IC between DT pin and GND, and it is not recommended to leave DT pin open.

Figure 32.Dead Time Setting

The falling edge of one input signal activates the the programmed dead time for the other signal. The dead time of the output signal is selected by IC, either the dead time set by IC itself or for the dead time of input signal itself, and the IC output chooses the longer one out of the two. If both input signals are high at the same time, both output signals are immediately set to low. This feature is intended to prevent shoot-through and does not affect the normal operation of the dead time settings. The following figure illustrates and demonstrates the various dead time logical operations.

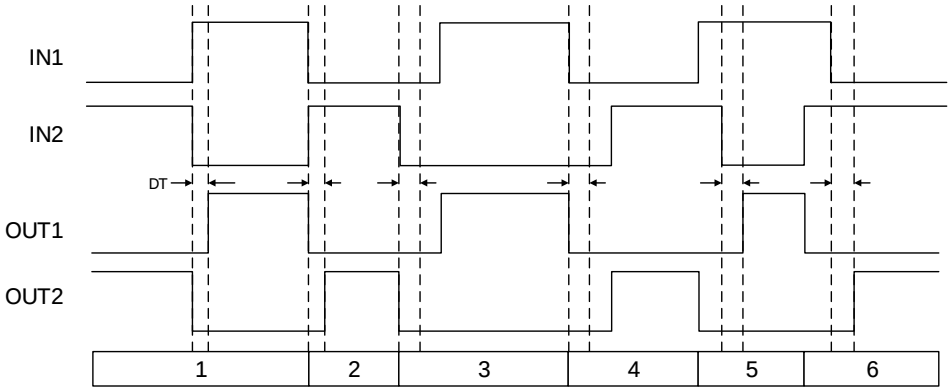


Figure 33. BTD21520M Input and Output Logic Relationship With Input Signals

State 1: IN2 goes low, IN1 goes high. IN2 sets OUT2 low immediately and assigns the programmed dead time to OUT1. OUT1 is allowed to go high after the programmed dead time.

State 2: IN2 goes high, IN1 goes low. Now IN1 sets OUT1 low immediately and assigns the programmed dead time to OUT2.OUT2 is allowed to go high after the programmed dead time.

State 3: IN2 goes low, IN1 is still low.IN2 sets OUT2 low immediately and assigns the programmed dead time for OUT1. In this case, the input signal's own dead time is longer than the programmed dead time. Thus, when IN1 goes high, it immediately sets OUT1 high.

State 4: IN1 goes low, IN2 is still low. IN1 sets OUT1 low immediately and assigns the programmed dead time to OUT2. IN2's own dead time is longer than the programmed dead time.Thus, when IN2 goes high, it immediately sets OUT2 high.

State 5: IN1 goes high, while IN2 and OUT2 are still high.To avoid overshoot, IN1 immediately pulls OUT1 low and keeps OUT1 low. After some time IN2 goes low and assigns the programmed dead time to OUT1. OUT2 is already low. After the programmed dead time, OUT1 is allowed to go high.

State 6: IN2 goes high, while IN1 and OUT1 are still high. To avoid overshoot, IN2 immediately pulls OUT1 low and keeps OUT2 low. After some time IN1 goes low and assigns the programmed dead time to OUT2. OUT1 is already low.After the programmed dead time, OUT2 is allowed to go high.

9.5.4 BTD21520E Dead Time

A dead time elapses before OUT1 or OUT2 goes high, so as to prevent the high and low side MOSFET shoot-through.

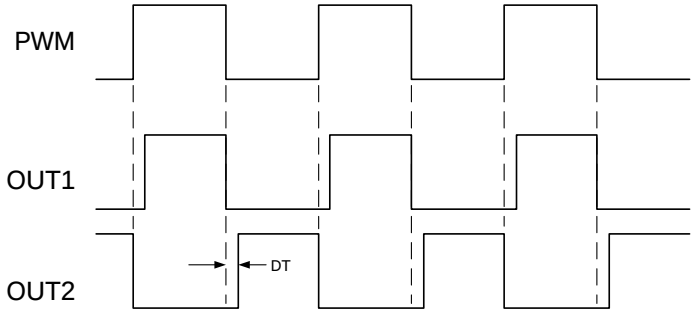


Figure 34. Logic relationship between input and output signals of BTD21520E

9.6 Protection Function

9.6.1 UVLO

There is an internal undervoltage lock-out (UVLO) on the power circuit function area between VDDx and VEE pins of two out-puts.When the voltage of VDDx is below the undervoltage recovery threshold before starting, or below the undervoltage protection threshold after starting, the output will remain low regardless of the input state. When the output of the driver is in powered-off or undervoltage state, its output is clamped to the low level by the active clamping circuit, as shown in the figure below.At this time, the PMOS of the high side is blocked and high impedance, and the NMOS gate of the low side is connected to the output of the driver by the resistor R_{CLAMP}.In the absence of bias voltage, the output is effectively clamped to the threshold voltage of the low-side NMOS device, typically around 1.5V (see Figure 35).

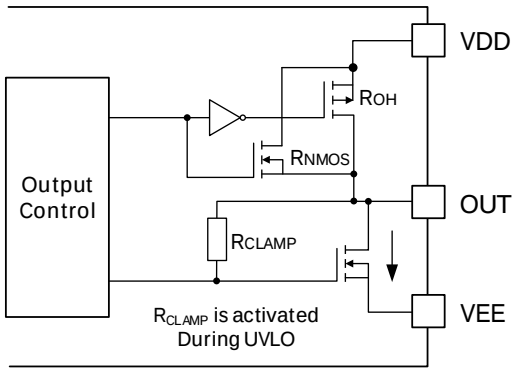


Figure 35. Simplified Representation of Active Pulldown Feature

The VDDx undervoltage protection has a V_{VDD_HYS} feature that prevents vibration in the presence of noise from the power supply to ground. This also allows the device to accept a small decrease in bias voltage when the device starts to turn on/off and the operating current consumption increases abruptly. Like the VDDx, there is also an undervoltage lock-out (UVLO) integrated on the primary side of the VCC.When the bias voltage is applied to the VCC terminal and the voltage is lower than the undervoltage turn-on threshold, the device will not be activated.After the activation of the device, if the VCC voltage continuously decreases to the undervoltage turn-off threshold, the signal will stop transmission.Like the undervoltage lockout of VDD, the undervoltage lockout of VCC also has hysteresis feature.

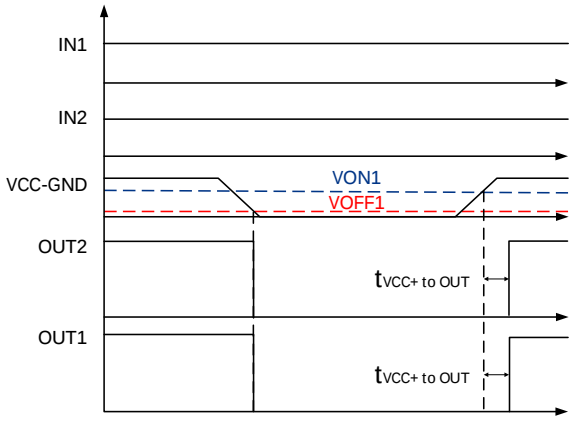


Figure 36. Timing Diagram of Undervoltage Lockout

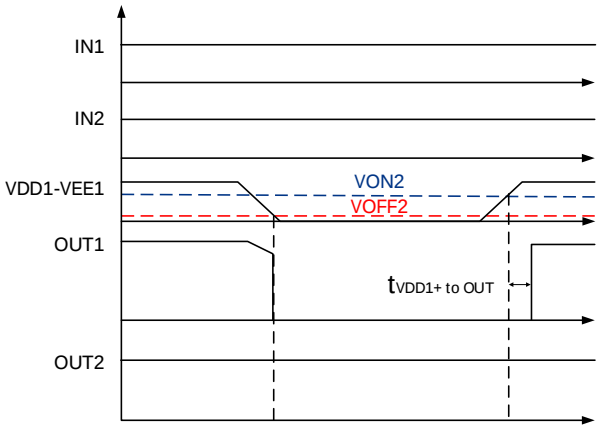


Figure 37. Timing Diagram of Undervoltage Lockout

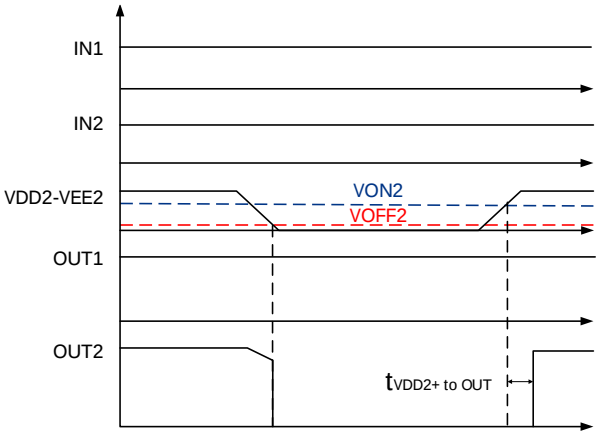


Figure 38. Timing Diagram of Undervoltage Lockout

9.7 ESD Structure

The figure below shows the ESD-protected diode configuration of the input and output pins.

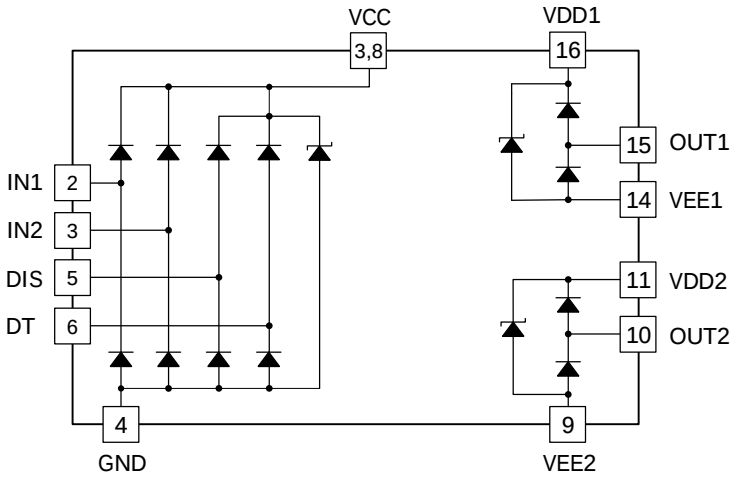


Figure 39. ESD Structure Diagram

10.Applications

The following sections introduce the basic typical application of the driver ICs, which is for reference only. In practical application, users need to verify and test its applicability according to their own design requirements to confirm the system function.

10.1 Typical Applications

It is recommended that customers add a RC filter with a small time constant at the input port to filter out high-frequency interference without adding a large delay. It is recommended that the resistance value should be between 0 and 100Ω and the capacitance should be less than 1000pF. When setting this parameter, the influence between high frequency interference and delay needs to be taken into account.

To ensure the supply stability, It is recommended to add an appropriate capacitor between the power supply and ground. It is recommended that the primary side supply VCC-GND be connected in parallel with 1uF+ 0.1uF capacitor C_{VCC}, and the secondary side supply VDDx-VEEx be connected with 10μF+ 0.22μF capacitors C_{VDD1} and C_{VDD2}.

The bootstrap capacitor is charged by VDD through an external bootstrap diode every cycle when the low side transistor turns on. Charging the capacitor involves high-peak currents, and therefore transient power dissipation in the bootstrap diode may be significant. Conduction loss also depends on the diode' s forward voltage drop. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver circuit.

The recommended value for R_{BOOT} is between 1 Ω and 20 Ω depending on the diode used.

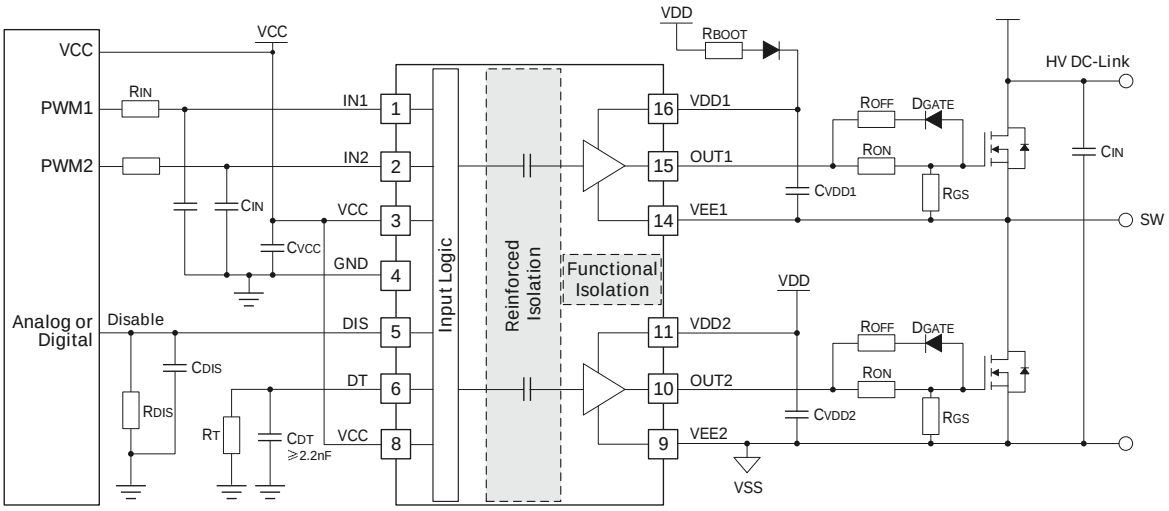


Figure 40. BTD21520M Application Diagram

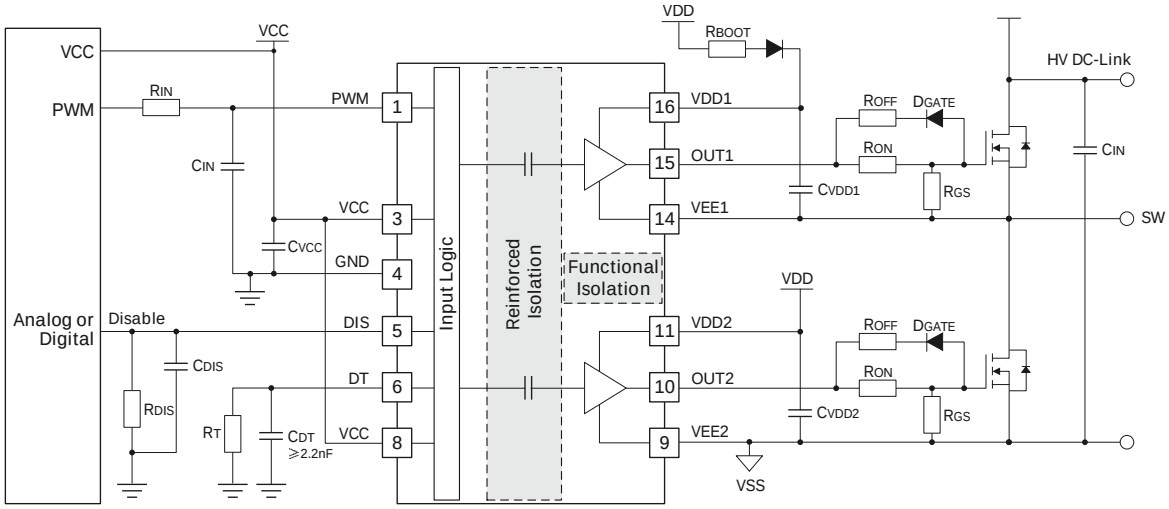


Figure 41. BTD21520E Application Diagram

10.2 Recommended Designs

10.2.1 Recommended Design of Secondary Side Supply

In order to avoid partial turn-on of the gate of the power device due to interference, it is recommended that customers add a negative supply when designing the driving output.It is recommended to use the following two methods to generate the negative supply: Use a regulator to generate stable negative voltage, or use both positive and negative supplies.

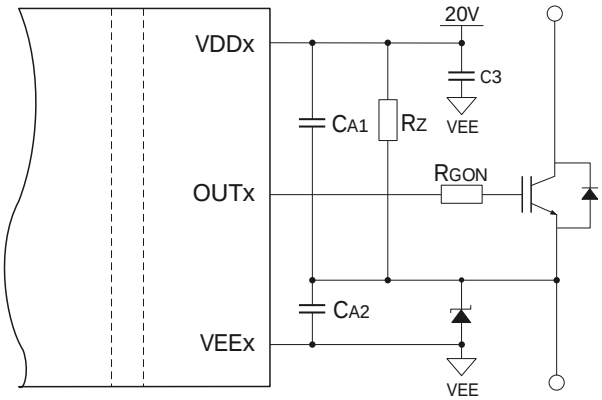


Figure 42. Voltage Regulator Design

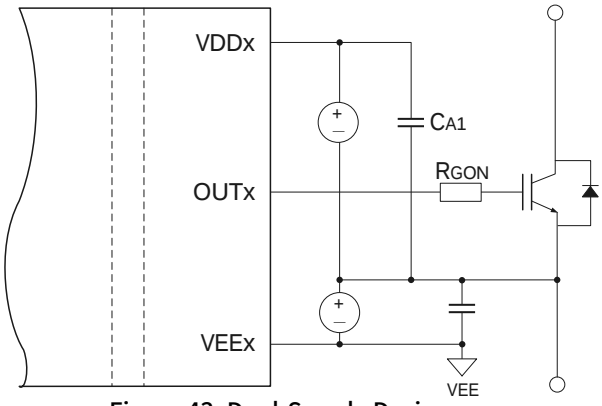
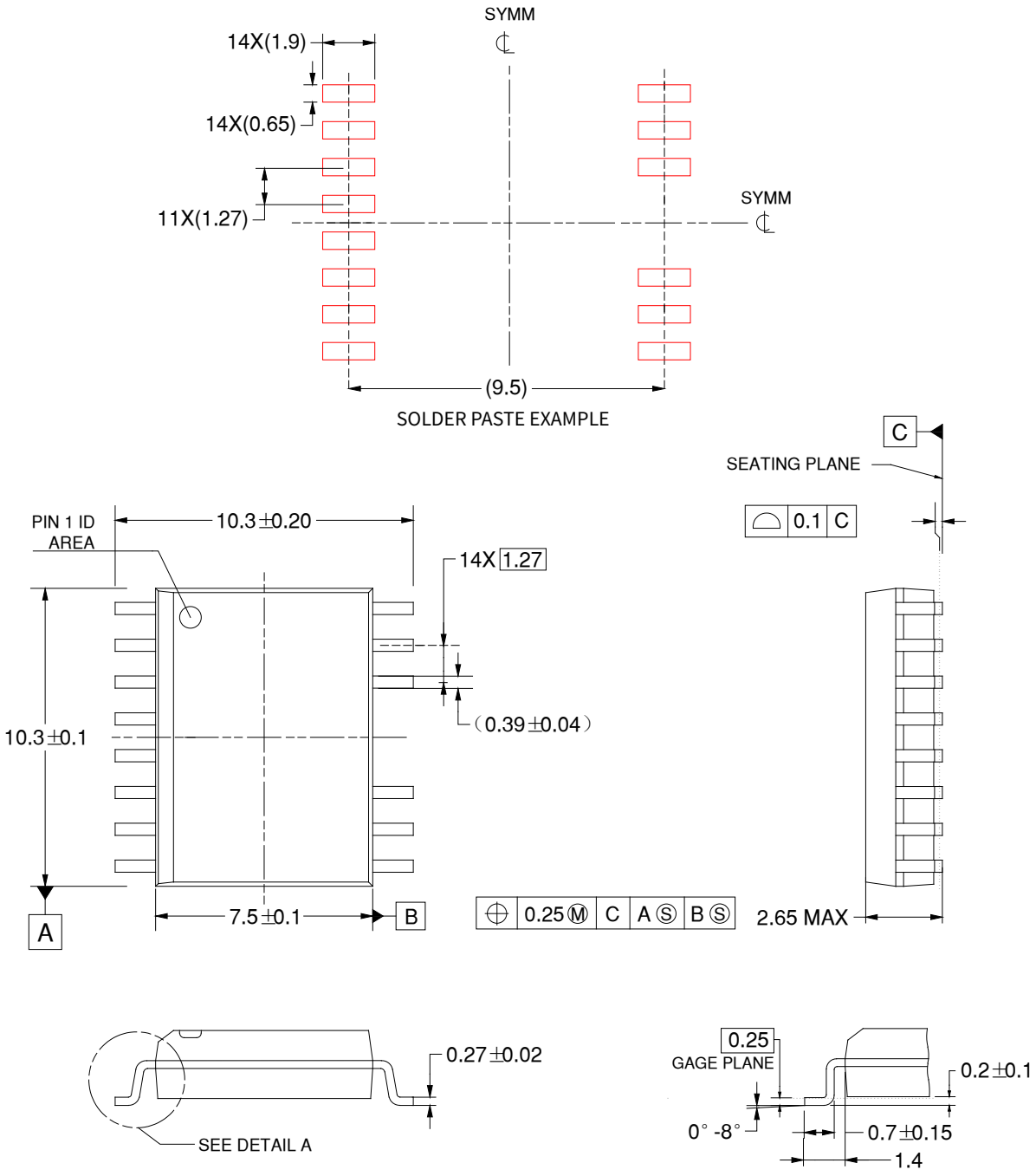


Figure 43. Dual-Supply Design

11.Packaging and Packing Information

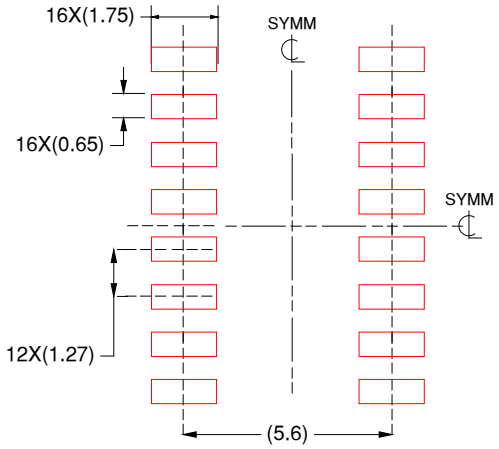
11.1 Package Identifier

11.1.1 SOW-14 Package Identifier

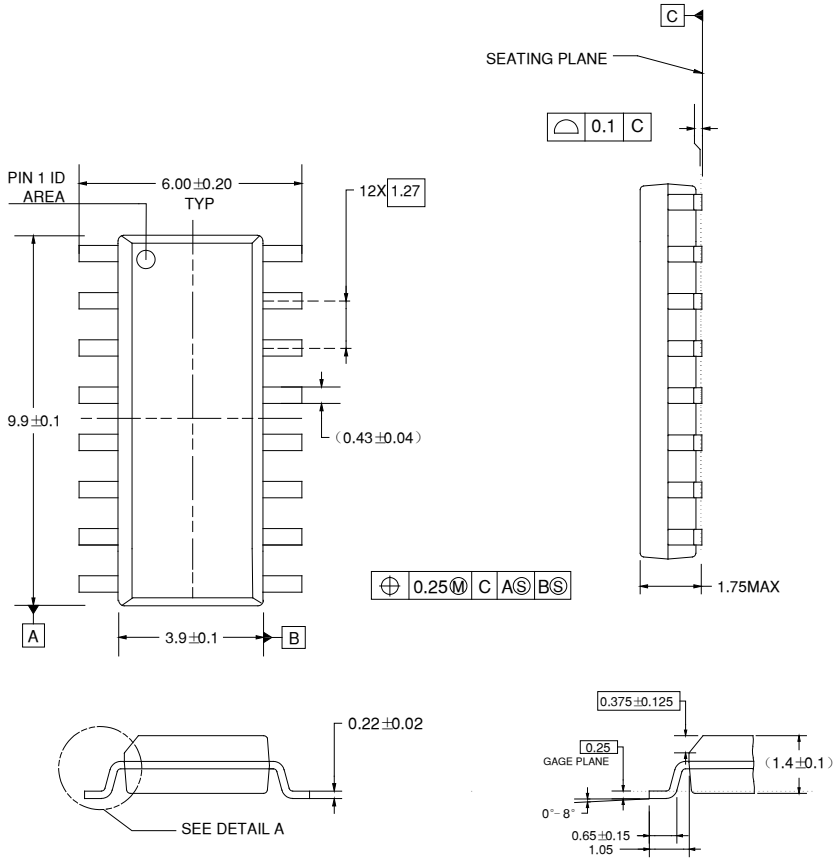


Note: 1)Legend unit: mm.

11.1.2 SOP-16 Package Identifier



SOLDER PASTE EXAMPLE



Note: 1) Legend unit: mm.

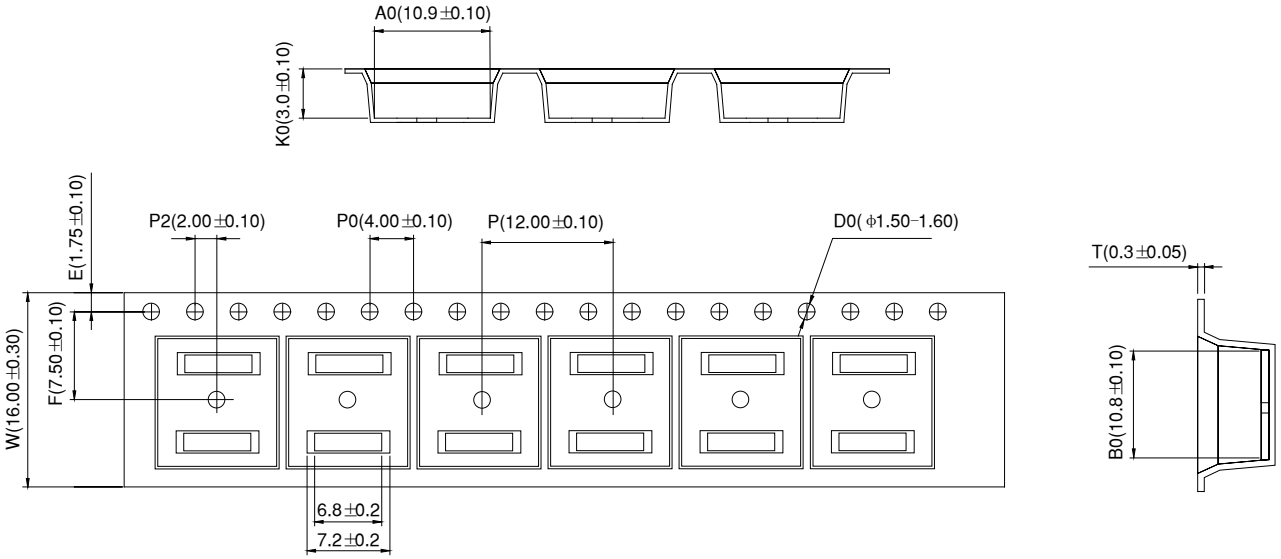
Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. It is recommended that all integrated circuits be handled with appropriate precautions.Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure.Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

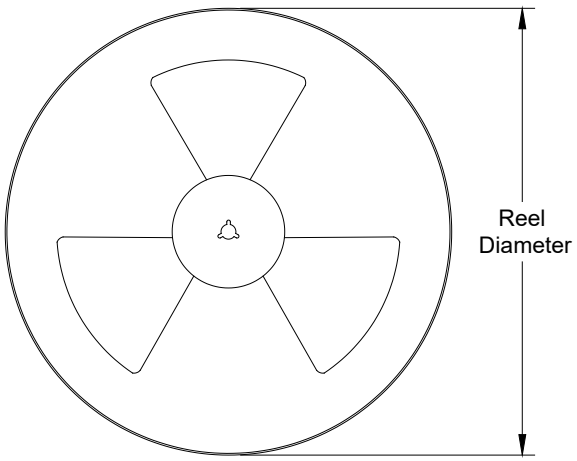
11.2 Packing Information

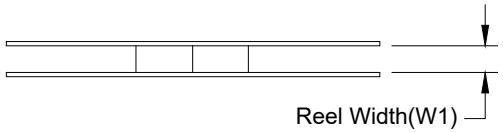
11.2.1 SOW-14 Packing Information



Note: 1) Legend unit: mm.

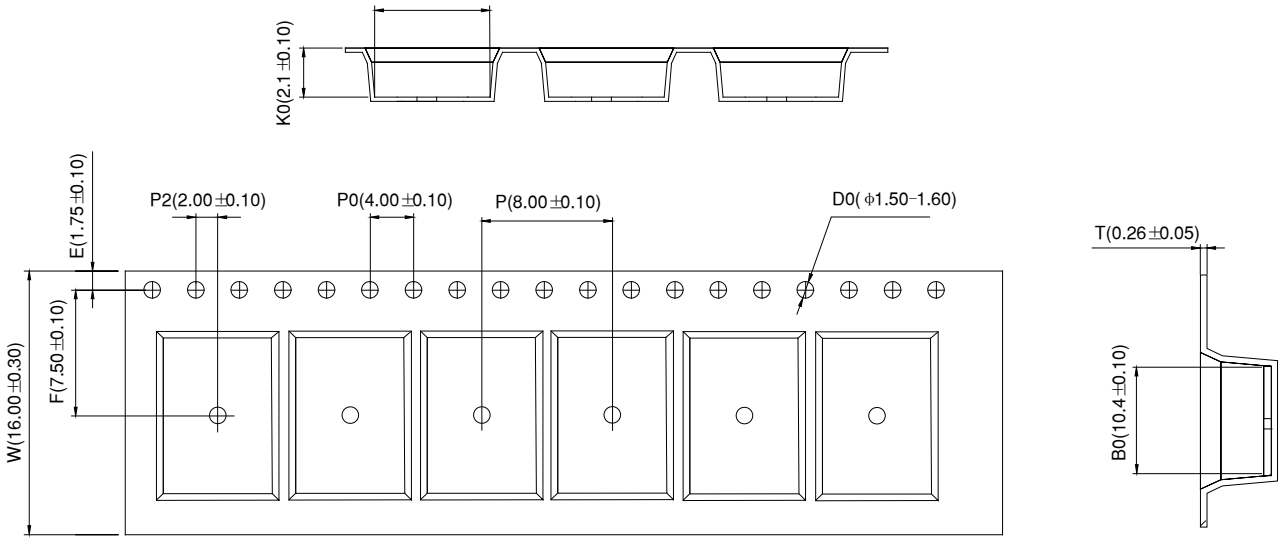
REEL DIMENSIONS





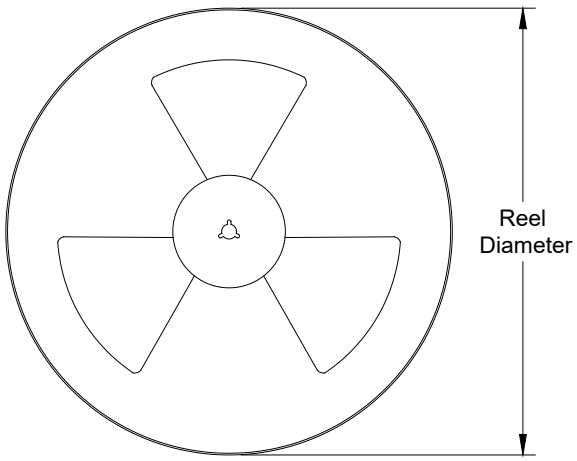
ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	12.4mm

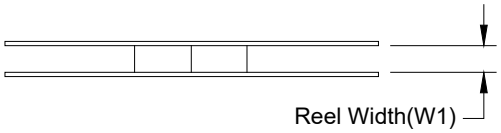
11.2.2 SOP-16 Packing Information



Note: 1) Legend unit: mm.

REEL DIMENSIONS





ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	16mm

12.Version Description

REVISION	NOTES	DATE
Rev.0.0	Released datasheet	12-Jan-2023
Rev.0.1	Parameters extended and SOP-16 package information added	15-Dec-2023
Rev.0.2	Safety certification added	28-Mar-2024

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